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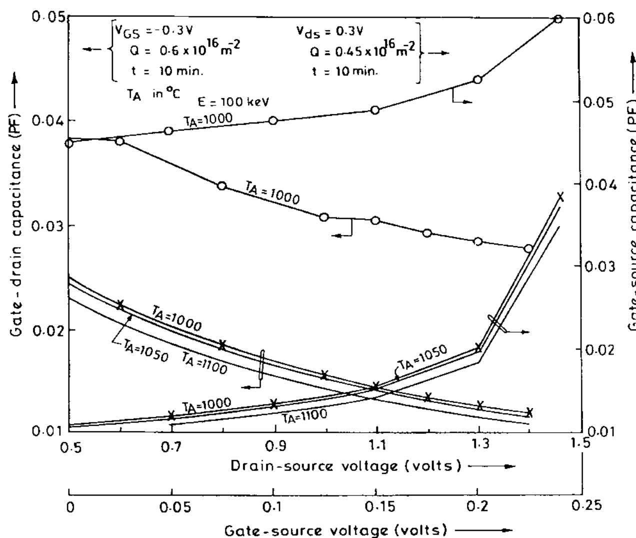


Fig. 2. The graph represents $C_{\rm gd} - V_{\rm ds}$ (axis on the left) and $C_{\rm gs} - V_{\rm gs}$ (axis on the right) for Phosphorous implantation at various anneal temperatures. Lines with circles are for Gaussian and with crosses are for calculated Pearson values.

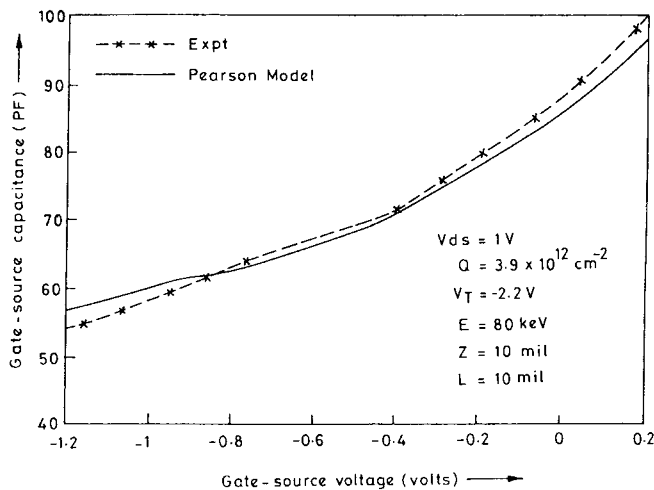


Fig. 3. Comparison with experimental data for phosphorous at $E = 80$ KeV.

source capacitance of our model is compared with the experiment data [1] (Fig. 3) and is in good agreement thus confirms the validity of this approach.

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# A Model for Thermal Growth of Ultrathin Silicon Dioxide in $O_2$ Ambient: A Rate Equation Approach

Suresh Gorantla, S. Muthuvenkatraman, and Rama Venkat

***Abstract*— A new thermal oxidation model based on a rate equation approach with concentration dependent diffusion coefficient is proposed for ultrathin $SiO_2$ for thicknesses of the order of 100 Å. The oxidation reaction of silicon is assumed to be dependent on the concentrations of unreacted silicon and oxygen. The results of oxide thickness versus oxidation time for various growth conditions and activation energies for diffusion coefficients are in agreement with various experimental data for $O_2$ ambient.**

## I. Introduction

Many theoretical [1]–[4] and experimental [5]–[8] studies have been devoted to this important area of IC processing since the early 1960's. The oxide growth model proposed by Deal and Grove (DG) [1] has been well accepted and utilized for thick oxide regime (>300 Å). Massoud *et al.* [2], [5] have studied ultrathin oxide growth for various orientations experimentally and have proposed a growth model which included an exponential term to the DG growth rate expression to account for the enhanced growth rate at small times. Murali *et al.* [3] have proposed a growth model for ultrathin oxide regime including lower resistance to diffusion during the initial phase of oxidation and allowing oxidation to occur over the thickness instead of at the interface. Thanikasalam *et al.* [4] proposed a model which suggested the formation of sub-stoichiometric oxide, SiO, as a precursor to the final product of $SiO_2$. The model assumes that oxidation proceeds via dissociative chemisorption of molecular oxygen.

In this article, a new model with transparent physics based on a rate equation approach is proposed for $O_2$ ambient for thermal oxidation of (100) Si. In this model concentration dependent diffusion coefficients are employed.

## II. Theory

### A. Mathematical Formulation

The thermal oxidation of silicon in $O_2$ ambient involves two kinetic processes, namely, the diffusion of oxygen through the $SiO_2$ and the chemical reaction

$$\mathrm{Si} + \mathrm{O_2} \rightleftharpoons \mathrm{SiO_2}. \quad (1)$$

The kinetics of the oxidation process can be mathematically formulated as follows. Firstly, let us partition the amorphous $SiO_2$ and Si into $n$ layers, for mathematical convenience. The thickness of a Si mono-layer is 1.358 Å, if fully unoxidized, and the average thickness of an $SiO_2$ mono-layer is 3.09 Å, if fully oxidized. The time evolution of oxygen and unreacted silicon concentrations ($C_{\rm O}$ and $C_{\rm Si}$, respectively) in the $n$th layer can be expressed as

$$\frac{\partial C_{\rm O}(n)}{\partial t} = D_{\rm O} \frac{\partial^2 C_{\rm O}(n)}{\partial x^2} - k_s C_{\rm O}(n) C_{\rm Si}(n) \quad (2)$$

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and

$$\frac{\partial C_{\rm Si}(n)}{\partial t} = -\frac{k_s C_{\rm O}(n) C_{\rm Si}(n)}{2} \tag{3}$$

where $C_{\rm O}(n)$ and $C_{\rm Si}(n)$ are the layer coverages of oxygen (O) and silicon (Si) atoms in the $n$th layer, respectively, with values in the range of 0 and 1. The value of $C_{\rm O}(n)$ is 1 when the number of O atoms in a layer is equal to $1.275 \times 10^{15}/\text{cm}^2$, which is the maximum for a square lattice packing of O atoms with ionic radius of 1.4 Å, and $C_{\rm O}(n)$ is equal to 0, when the layer has no O atoms. For Si, $C_{\rm Si}(n)$ was computed based on the atomic arrangement in the (100) plane of a diamond cubic structure. Thus, $C_{\rm O}(n)$ and $C_{\rm Si}(n)$ are dimensionless quantities. $D_{\rm O}$ is the diffusion coefficient of O atoms and $k_s$ is the reaction rate constant for reaction given by (1). The model adopted in (3) is a deviation from the previous models, in which it was assumed that $C_{\rm Si}(n) = 1$. The first term on the RHS of (2) is the diffusion term, and the second term represents the loss due to reaction. The factor 2 in (3) accounts for the fact that for every Si atom two O atoms are consumed in the oxidation process, thus maintaining the stoichiometry of $SiO_2$. The two differential equations given by (2) and (3) must be solved, subject to the conditions

$$C_{\rm O}(n)|_{t=0} = C_{\rm SO}, \quad \forall n = 1, 2, 3 \tag{4}$$

$$C_{\rm O}(n)|_{t=0} = 0, \quad \forall n = 4, 5, 6 \cdots \tag{5}$$

and

$$C_{\rm Si}(n)|_{t=0} = 0, \quad \forall n = 1, 2, 3 \tag{6}$$

$$C_{\rm Si}(n)|_{t=0} = 1, \quad \forall n = 4, 5, 6 \cdots \tag{7}$$

Physically, $C_{\rm SO}$ is the layer coverage of O atoms in the solid-vapor interface. $C_{\rm SO}$ is expected to be directly proportional to the partial pressure of $O_2$ and inversely proportional to the temperature based on Boyle's law. To convert the concentration of O atoms at the surface from atoms/cm$^3$, obtained from the Boyle's law, to layer coverage, we assumed a square lattice of O atoms with interatomic distance of 2.8 Å and the layer thickness is equal to 2.8 Å. The square lattice allows a maximum of $1.275 \times 10^{15}$ atoms/cm$^2$ which corresponds to $C_{\rm SO}^{\rm max} = 1$. Using this value of maximum number of atoms as a normalizing factor, we obtain $C_{\rm SO} = (k/T)p_{\rm O_2}$, where $k = 0.322\,38°$ K/atm, $T$ is the temperature in °K, and $p_{\rm O_2}$ is the partial pressure of $O_2$ in atm. It is noted that $n$ in (4) represents the gaseous phase layer at the surface and can be arbitrarily larger than 3 to accommodate proper numerical integration.

The $D_{\rm O}$ is assumed to be the same in both Si and $SiO_2$. The $D_{\rm O}$ and $k_s$ are given by

$$D_{\rm O} = D_{\rm O}^{of}(1 - C_{\rm O})^p e^{-E_{D_{\rm O}}/k_B T} \tag{8}$$

and

$$k_s = k_s^o e^{-E_k/k_B T} \tag{9}$$

where $E_{D_{\rm O}}$ is the activation energy for diffusion of O through the oxide, and $E_k$ is the activation energy for the chemical reaction given by (1). $D_{\rm O}^{\rm of}$ is the frequency factor for diffusion of O and $k_s^o$ is the frequency factor for the chemical reaction given by (1). $k_B$ is the Boltzmann constant and $T$ is the temperature in $^o$ K. Additionally, the frequency factors for the diffusion coefficients are assumed to have power law dependence on the concentration of unreacted oxygen in the $SiO_2$ and Si layers. The physical reason for assuming a power law dependence is as follows. The more the concentration of O, the greater will be the blocking of the interstitial diffusional paths in the $SiO_2$ network and Si crystal by these atoms, thereby, reducing the concentration of oxidizing species available for oxidation.

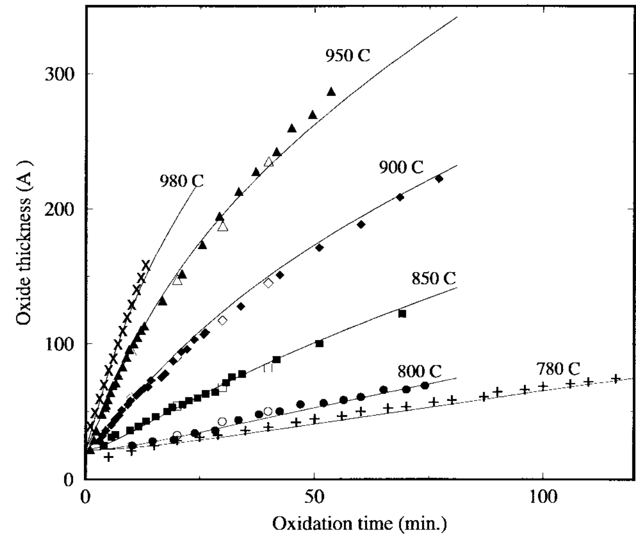


Fig. 1. Plots of oxide thickness as a function of oxidation time for various temperatures in $O_2$ ambient, along with experimental data of Massoud *et al.* [1] (filled symbol), Chao *et al.* [6] (open symbol), and Irene *et al.* [7] ($+$, $\times$ symbols).

The differential equations are solved numerically using the fourth order Runge Kutta technique. To obtain the unknown model parameters $D_{\rm O}^{of}, k_s^o, E_{D_{\rm O}}$, and $p$, experimental oxide thickness versus time data with 1 atm $p_{\rm O_2}$ for two temperatures (800 °C and 950 °C) of Massoud *et al.* [5] were fitted to our theoretical results. The fitted values of the activation energies and frequency factors are $E_{D_{\rm O}} = 1.75$ eV, $E_k = 2.26$ eV, $D_{\rm O}^{of} = 1.05 \times 10^{-7}$ cm$^2$/s., $k_s^o = 3.92 \times 10^7$/s., and $p = 1$. These values were employed to obtain the rest of the data. An initial native $SiO_2$ of thickness 20 Å is assumed for all our data.

## III. Results and Discussion

Plots of oxide thickness versus time in $O_2$ ambient are shown in Fig. 1. along with the experimental data of Massoud *et al.* [5], Chao *et al.* [6], and Irene *et al.* [7] for growth with 1 atm $O_2$ and temperatures in the range of 800–1000 °C. The agreement between the theoretical results and the three sets of experimental data is good for all growth conditions and thicknesses. The initial rapid increase in growth thickness with time is due to higher $D_{\rm O}$ resulting from smaller blocking effect by lower $C_{\rm O}$. As the time increases, the $C_{\rm O}$ increases and hence, $D_{\rm O}$ decreases leading to the saturation of growth rate due to low availability of O for the oxidation reaction given by (1).

In the $O_2$ ambient, the activation energy of 2.26 eV for oxidation reaction obtained is close to the Si-Si bond energy (1.86 eV) and is in close agreement with the values reported by Deal and Grove model [1], which is 2.0 eV. The activation energy for $SiO_2$ reaction should be larger than the Si-Si bond energy. The diffusion activation energy, $E_{D_{\rm O}}$, of 1.75 eV obtained from our model is comparable to 1.24 eV reported by Deal and Grove [1].

Our model shows that there is a finite width of a few nm to the Si-$SiO_2$ interface, which is in agreement with Rosencher *et al.* [9]. The model does not provide analytical solutions. It does not include any influence of stress on the growth behavior. The stress is expected to influence the diffusion coefficient.

## IV. Conclusion

A simple thermal oxidation model for ultrathin oxide regime based on the rate-equation approach is presented. Theoretical results are

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in excellent agreement with experimental work of various research groups [5]–[7] for a variety of growth conditions with temperatures in the range of 780–1100 °C for $O_2$ ambient (1 atm). The activation energies for $O_2$ ambient, diffusion and oxidation reactions obtained in this work compares well with the experimental work [1]. The model is general and is expected to be suitable for other orientations, oxidation in $N_2O$ ambient, and Si nitridation with change in the model parameter values.

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# Integration of InAlAs/InGaAs/InP Enhancement- and Depletion-Mode High Electron Mobility Transistors for High-Speed Circuit Applications

A. Mahajan, P. Fay, M. Arafa, and I. Adesida

***Abstract*— A process for the monolithic integration of enhancement- and depletion-mode high electron mobility transistors (E/D-HEMT's) on InAlAs/InGaAs/InP is reported. The E-HEMT's with a 1.0-$\mu$m gate length exhibit a threshold voltage of $+255$ mV and a maximum dc extrinsic transconductance of 503 mS/mm at room temperature, while a threshold voltage of $-317$ mV and a transconductance of 390 mS/mm are measured for the D-HEMT's of the same gate length. The devices show excellent RF performance, with a unity current-gain cutoff frequency $(f_t)$ of 35 GHz and a maximum frequency of oscillation $(f_{\max})$ of 95 GHz for both the E- and D-HEMT's. To the best of the authors' knowledge, this is the first demonstration of an E/D-HEMT technology on lattice-matched InP that is suitable for circuit integration.**

## I. INTRODUCTION

The development of monolithically integrated enhancement- and depletion-mode high electron mobility transistors (E/D-HEMT's) on lattice-matched InP is of considerable interest for high-speed, low-power communication systems [1], [2]. Circuits utilizing such an E/D technology offer several advantages over circuits employing a conventional D-mode only technology. With an E/D technology, dc level shifting stages can be eliminated between successive amplifier gain stages, thus reducing the number of transistors in the circuit, and hence saving valuable chip area. This elimination of level shifting stages also leads directly to a reduction in the power consumption of the circuit. In addition, it is possible to utilize a single power supply for circuits realized in an E/D technology which is cumbersome to implement in circuits using only conventional D-HEMT's. However, the development of E-HEMT's on InP has been limited by the inability to achieve sufficiently large gate Schottky barrier heights on InAlAs [3]. Recently, a barrier height of 1.09 eV has been reported for Pt on InAlAs [4], making Pt an excellent candidate for a gate metal for E-HEMT's. Consequently, high-performance InP-based E-HEMT's have been demonstrated using the buried Pt gate technique [5], [6].

In this brief, we demonstrate the monolithic integration of InAlAs/InGaAs/InP E- and D-HEMT's that is suitable for circuit applications. The InP-based E- and D-HEMT's fabricated here exhibit excellent dc and RF performance. Additionally, the E-HEMT's exhibit a threshold voltage standard deviation of only 7 mV for an 80-device sample size while the D-HEMT's show a 12-mV standard deviation for the same sample size. These small variations in threshold voltage, combined with the excellent electrical performance make this device technology a suitable candidate for use in high-speed, low-power, large-scale integrated circuits.

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