On High-Performance Parallel Decimal Fixed-point Multiplier Designs

Ming Zhu  zhum2@unlv.nevada.edu
Dept. of Electrical and Computer Engineering, UNLV

Introduction

Decimal computations are required in finance, and etc.

- Precise representation for decimals (E.g. 0.2, 0.7...) 
- Performance Requirements (Software simulations are very slow)

Traditional Approach (8421 BCD)

$$P_{2n} = A_n \times B_n$$

$$= A_n \left( \sum_{i=0}^{n-1} b_i (10)^i \right)$$

$$= \sum_{i=0}^{n-1} A_n b_i (10)^i$$

$$= \sum_{i=0}^{n-1} P_{Ai} (10)^i$$


My Architecture (8421-5421 BCD)

$$P_{2n} = A_n \times B_n = \sum_{i=0}^{n-1} A_n b_i (10)^i$$

$$= \sum_{i=0}^{n-1} A_n (b_0 + b_1) (10)^i$$

$$= \sum_{i=0}^{n-1} (A_n b_0) + A_n b_1 (10)^i$$

$$= \sum_{i=0}^{n-1} (P_{Ai} b_0) + P_{Ai} b_1 (10)^i$$

$$b_i = 5 \times b_i \times (-1)^{OP} b_i$$

$$b_i \in \{0, 1, 2\}, OP \in \{0, 1\}$$

Evaluation Results

Conclusion:
- Best designs in terms of delay and delay-area product.
- Simplified logic of PPG with 8421-5421 recoding.
- 8421 CLAs organized as tree structure for PPA
- Could be pipelined for higher data throughput and hardware utilization