On High-Performance Parallel Decimal Fixed-point Multiplier Designs

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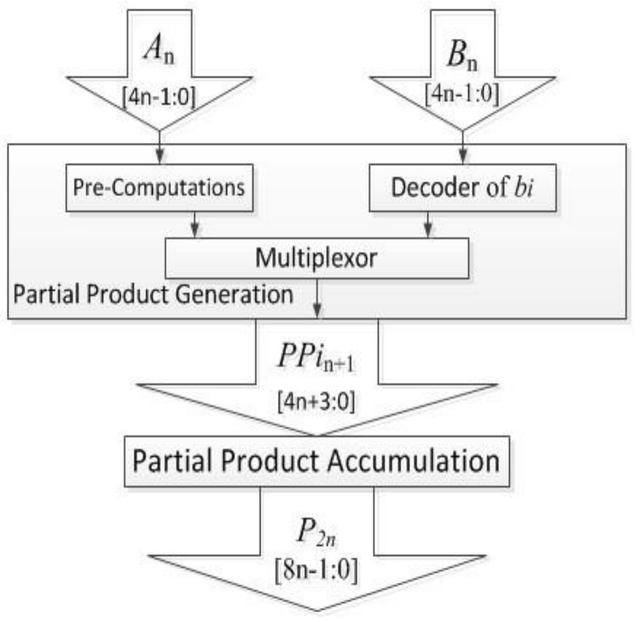
Introduction

Decimal computations are required in finance, and etc.

- Precise representation for decimals (E.g. 0.2, 0.7…)
- Performance Requirements (Software simulations are very slow)

Traditional Approach (8421 BCD)

$$P_{2n} = A_n \times B_n$$
$$= A_n(\sum_{i=0}^{n-1} b_i(10)^i)$$
$$= \sum_{i=0}^{n-1} A_n b_i(10)^i$$
$$= \sum_{i=0}^{n-1} PPi_{n+1}(10)^i$$



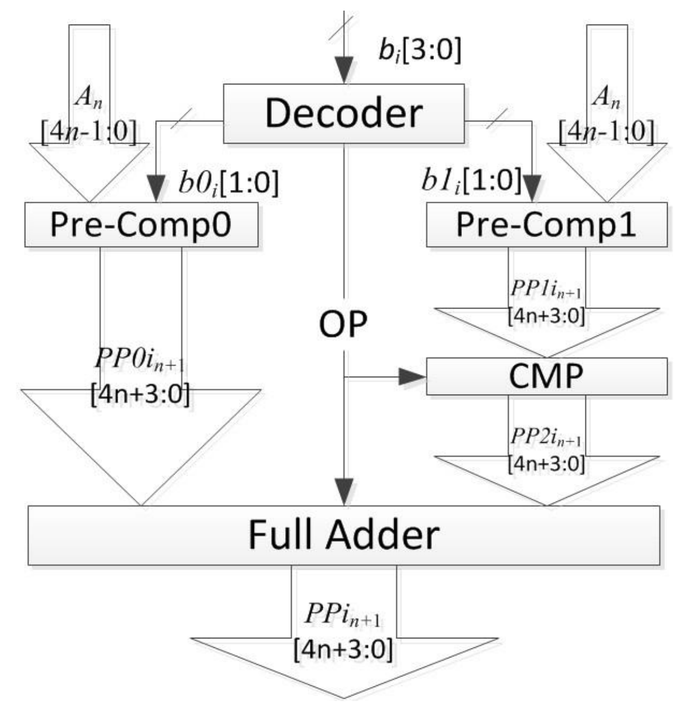
$$\begin{array}{rcccccc} & & a_3 & a_2 & a_1 & a_0 \\ \times & & & & & b \\ \hline & & pt_3 & pt_2 & pt_1 & pt_0 \\ + & c_3 & c_2 & c_1 & c_0 & \\ \hline & pp_4 & pp_3 & pp_2 & pp_1 & pp_0 \end{array}$$

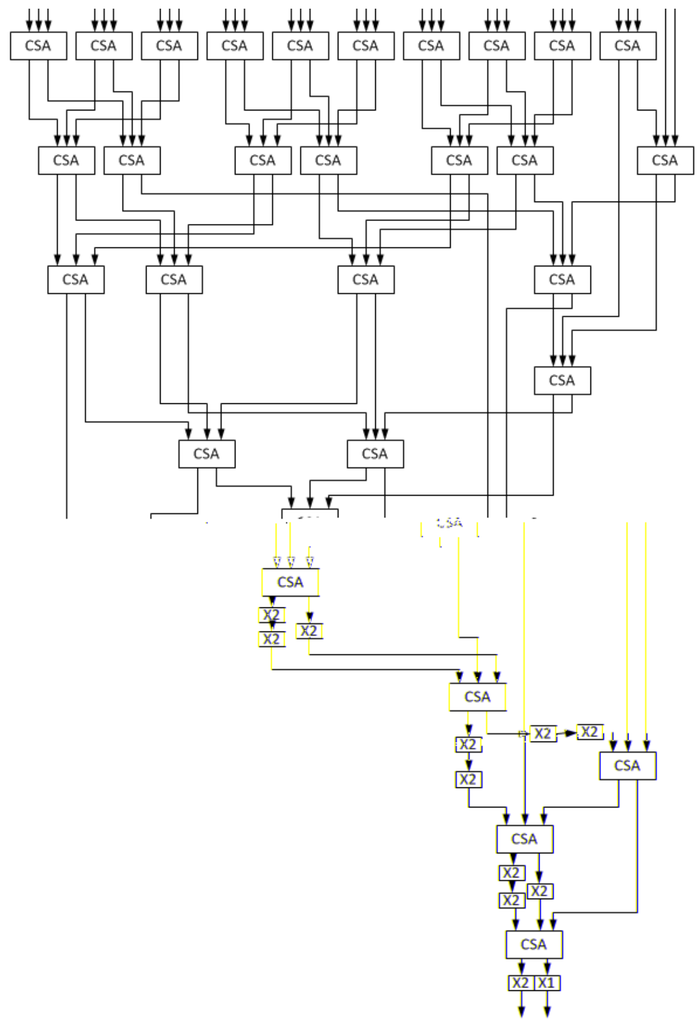
A	0010 0101 0111 0101
B	+0011 0100 0010 1000
Sum 1	0101 1001 1001 1101
Correction 1	+0000 0000 0000 0110
Sum 2	0101 1001 1010 0011
Correction 2	+0000 0000 0110 0000
Sum 3	0101 1010 0000 0011
Correction 3	+0000 0110 0000 0000
Result	0110 0000 0000 0011

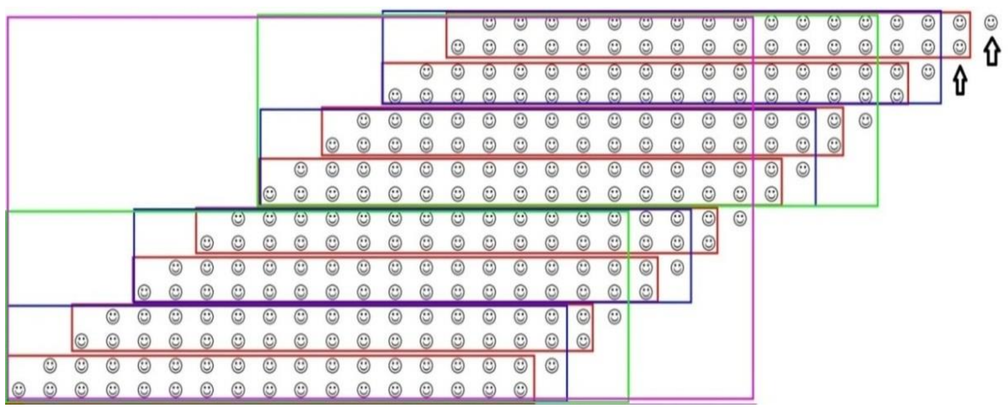
My Architecture (8421-5421 BCD)

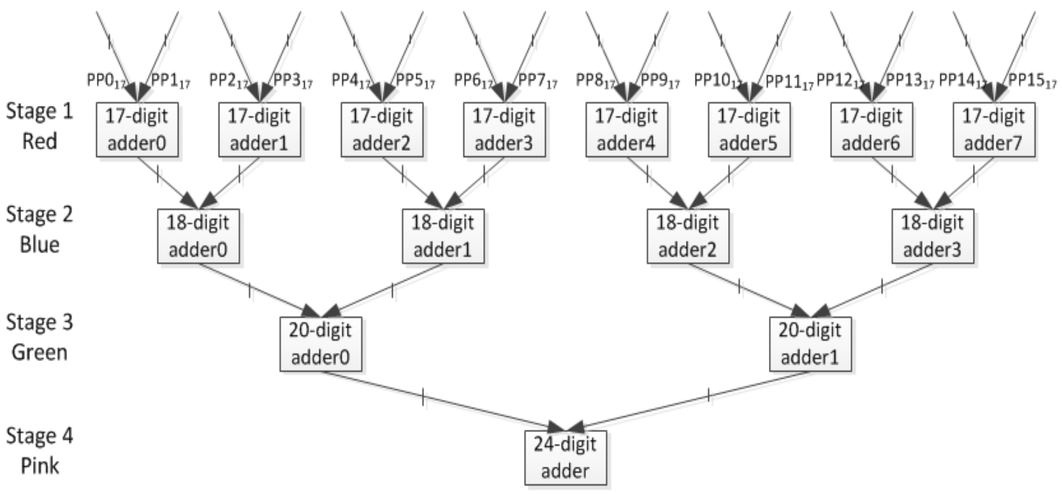
$$P_{2n} = A_n \times B_n = \sum_{i=0}^{n-1} A_n b_i(10)^i$$
$$= \sum_{i=0}^{n-1} A_n(b0_i + b1_i)(10)^i$$
$$= \sum_{i=0}^{n-1} (A_n(b0_i) + A_n(b1_i))(10)^i$$
$$= \sum_{i=0}^{n-1} (PP0i_{n+1} + PP1i_{n+1})(10)^i$$

$$b_i = 5 \times b_{iH} + (-1)^{OP} b_{iL}$$
$$b_{iH}, b_{iL} \in \{0,1,2\}, OP \in \{0,1\}$$









Conclusion:

- Best designs in terms of delay and delay-area product.
  - Simplified logic of PPG with 8421-5421 recoding.
  - 8421 CLAs organized as tree structure for PPA
- Could be pipelined for higher data throughput and hardware utilization

Evaluation Results