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David Albin and Joseph del Cueto

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# Correlations of Capacitance-Voltage Hysteresis with Thin-film CdTe Solar Cell Performance During Accelerated Lifetime Testing

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**Abstract**—In this paper we present the correlation of CdTe solar cell performance with capacitance-voltage hysteresis, defined presently as the difference in capacitance measured at zero-volt bias when collecting such data with different pre-measurement bias conditions. These correlations were obtained on CdTe cells stressed under conditions of 1-sun illumination, open-circuit bias, and an acceleration temperature of approximately 100 °C.

**Keywords**- Photovoltaic, Cadmium Telluride (CdTe), Capacitance Voltage Hysteresis, Transient Ion Drift (TID), Transient Capacitance, Deep Level Transient Spectroscopy (DLTS).

## I. INTRODUCTION

Polycrystalline CdS/CdTe thin film solar cells have demonstrated small-area, laboratory efficiencies of 16.5% [1]. The highest reported efficiency for CdTe modules in [2] is 10.9% though this value is nearly a decade old. Higher performance levels for industrial products based on CdTe are likely but not openly disseminated for strategic reasons. In addition to considerable research addressing efficiency, recent work has focused on the intrinsic durability of these thin film semiconductor devices. The effects of back contact and doping strategies have been heavily researched for example [3, 4, 5]. This is driven by the inherent difficulty in fabricating ohmic contacts on wide band gap, p-type CdTe. More recently, the detrimental effects of localized shunts [6], the general effects of polycrystalline thin film micro-nonuniformities [7], and cell fabrication details revealed through factorial, design-of-experiment research [8] have been openly presented.

The basic structure of a thin film CdS/CdTe solar cell is that of a glass superstrate design in which light passes through a conducting/insulating (buffer) oxide film layer stack deposited on glass. Most laboratory and industrial cells use tin-oxide (SnO<sub>2</sub>) for these layers, though there is considerable interest in more advanced stannate materials (Cd<sub>2</sub>SnO<sub>4</sub> and ZnSnO<sub>x</sub>). Once transmitted through the glass/TCO/buffer superstrate, light is then absorbed in the n-CdS/p-CdTe heterojunction structure which provides the field necessary for separating photo-generated carriers. A back contact structure completes the cell. A schematic of this basic design is shown in Figure 1.

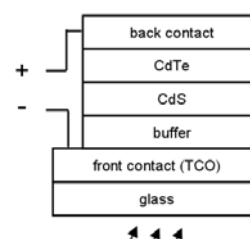


Fig. 1. Basic CdS/CdTe Solar Cell Design.

In order to ascertain the long term reliability of modules based upon CdS/CdTe, cells of this basic design were exposed to 1-sun illumination under open-circuit,  $V_{oc}$ , bias and acceleration temperatures of 60 – 120 °C for times exceeding 1000 hours [9]. Under field-use conditions, series-connected cells nominally see voltages somewhat less than  $V_{oc}$ , thus, open-circuit conditions represent an additional form of acceleration. In this study, two dominant degradation mechanisms were identified in the temperature range studied. As shown in Fig. 2(a), between 60-80 °C, an activation energy of 2.94 eV was measured and was attributed to S-outdiffusion from the CdS layer into the CdTe based upon a reported value of 2.8 eV for bulk diffusion of S in CdTe [10]. This assertion was also based upon the observation of Kirkendall-like voiding of the CdS layer in cells that underwent stress. In the temperature range 100-120 °C, an activation energy of 0.63 eV was determined which agreed well with the reported value of 0.67 eV for Cu diffusion in CdTe [11].

Since cell efficiency,  $\eta\%$ , is determined by the equation:

$$\eta\% = \frac{V_{oc} \times J_{sc} \times FF}{\Phi_{inc}} \quad (1)$$

(where  $\Phi_{inc}$ , the incident power density is typically normalized to a solar value of 100 mW/cm<sup>2</sup>), a correlation analysis  $\Delta\eta\%$  versus changes in  $V_{oc}$ , short-circuit current density,  $J_{sc}$ , and fill factor, FF, during stress testing as a function of stress temperature was performed. This analysis is shown in Figure 2(b).

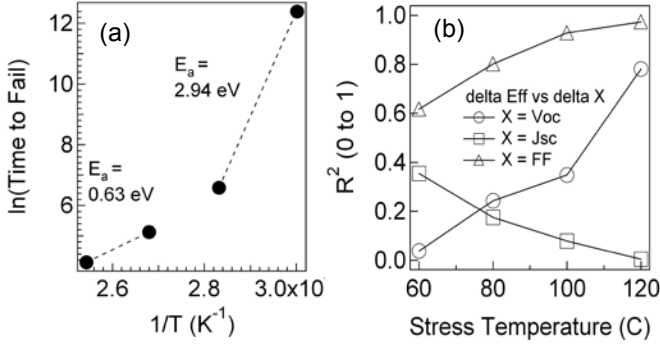


Fig. 2. Degradation activation energies (a) and correlation analysis (b) of how efficiency (Eff) changes versus changes in  $V_{oc}$ ,  $J_{sc}$ , and FF.

The moderate correlation of  $\eta\%$  with  $J_{sc}$  seen at lower stress temperatures is due to reduced optical attenuation associated with S-outdiffusion from the CdS. The most important variable affecting  $\eta\%$  at all temperatures, approaching a near ideal correlation at 120 °C, was FF. FF represents the efficiency by which photons absorbed in a solar cell are collected by a combination of field and diffusion-limited collection mechanisms. Within the space-charge, photo-generated electrons and holes are swept towards the n and p-sides of the junction respectively by the built-in field. In the quasi-neutral region, carrier diffusion length determines whether they are collected. Recombination of carriers before collection is the greatest impediment to improving the overall performance, primarily  $V_{oc}$ , for these cells.

The fundamental current-density,  $J$ , and voltage,  $V$ , behavior of a solar cell is represented by:

$$J = J_{SCR} + J_{QNR} + \left( \frac{V - JR_s}{R_{sh}} \right) - J_{ph} \quad (2)$$

where  $J_{SCR}$ ,  $J_{QNR}$ , and  $J_{ph}$  represent recombination currents in the space-charge and quasi-neutral regions of the cell, as well as the photo-generated current, while  $R_s$  and  $R_{sh}$  represent series and parallel (shunt) resistance losses.  $J_{SCR}$  and  $J_{QNR}$  are further represented by the following:

$$J_{QNR} = J_{01} \left( e^{\frac{q(V - JR_s)}{kT}} - 1 \right) \quad (3)$$

$$J_{SCR} = J_{02} \left( e^{\frac{q(V - JR_s)}{2kT}} - 1 \right) \quad (4)$$

where  $J_{01}$  and  $J_{02}$  are further dependent upon minority carrier transport properties.

In the fourth quadrant, maximum power output is achieved by maximizing the term,  $J_{ph}$ , and minimizing the first three terms in (2), often referred to collectively as the “forward” current. Each of the forward current terms contributes to decreased cell performance. It should be noted that the

recombination currents,  $J_{QNR}$ , and  $J_{SCR}$  are themselves dependent upon resistive effects as shown in (3) and (4).

The loss parameters  $J_{QNR}$ ,  $J_{SCR}$ ,  $R_s$ , and  $R_{sh}$  can be determined graphically or by direct modeling with programs like Pspice. Using the latter approach, the percent contribution each parameter contributes to the forward current (and thus loss) in the power quadrant for a laboratory made 14.4% CdS/CdTe solar cell is shown in Fig. 3.

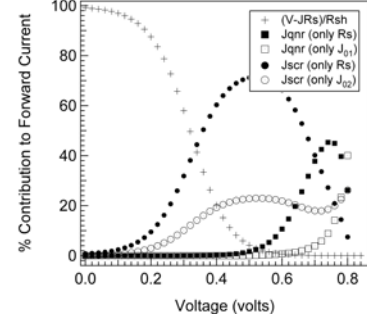


Fig. 3. Percent contribution to forward current losses modeled for a 14.4% CdS/CdTe cell.

The results shown in Fig. 3 use a model-fitted value of 3 ohms\*cm<sup>2</sup> for  $R_s$  which is a reasonable upper value observed during stress testing of these cells [9]. As seen in this figure, recombination occurs mostly in the space-charge except near  $V_{oc}$  where recombination in the quasi-neutral region, i.e., between the depletion width and back contact begins to dominate. Note that resistive contributions for both effectively go to zero at  $V_{oc}$  where  $J = 0$  in equations (3) and (4).

The effect of addressing recombination within the quasi-neutral region is shown in Fig. 4.

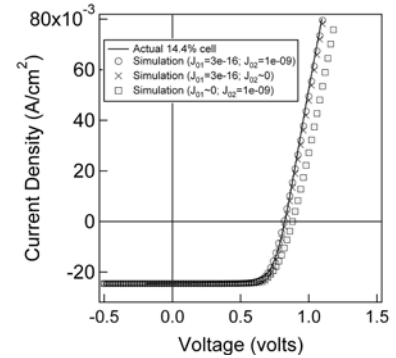


Fig. 4. The effect of reducing quasi-neutral recombination on the  $V_{oc}$  of CdTe solar cells (all  $J$  terms given in  $A/cm^2$ ).

Shown in this figure is the Pspice model simulation used to extract the loss mechanisms shown in Fig. 3 along with actual cell data in a conventional J-V diagram. In this case  $J_{01}$  and  $J_{02}$  equal  $3e^{-16}$  and  $1e^{-09}$   $A/cm^2$  respectively. Having obtained a good fit, the model is then perturbed by simulating conditions where recombination is removed in either the space-charge ( $J_{02} \sim 0$ ) or quasi-neutral ( $J_{01} \sim 0$ ) regions. As can be deduced from Fig. 4, improving CdTe material quality within the depletion width (space-charge) does not improve cell performance. However, an additional 60 mV (0.82 to 0.88) can result if recombination in the quasi-neutral region is reduced.

The results of this fundamental calculation make understanding the depletion width position important when determining why FF changes during stress testing of cells. With this goal in mind, a new technique for collecting capacitance-voltage (C-V) data quickly during accelerated stress testing was developed [12]. This technique collects capacitance data first in a reverse direction (rev) voltage scan followed by a subsequent, forward direction (fwd) scan. This approach yields two distinct C-V curves as shown in Fig. 5 for representative cells with and without Cu added intentionally as a dopant during back contact fabrication.

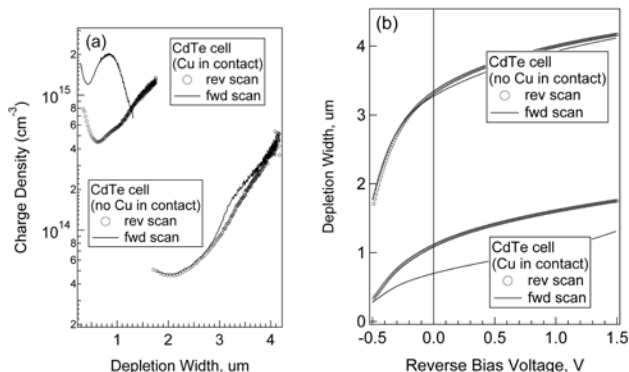


Fig. 5. Mott-Schottky plot (a) and corresponding depletion width vs. bias diagram (b) for CdS/CdTe cells with and without intentional Cu.

Fig. 5(b) clearly shows how Cu affects the space-charge depletion width,  $W_d$ . The strong decrease in  $W_d$  with Cu reflects an obvious increase in ionized acceptors,  $N_a^-$  in the CdTe possibly as  $Cu_{Cd}$  or as a paired, defect complex [13]. The decrease in  $W_d$  (since it can be so easily explained by doping) is not surprising. What is less obvious is the large degree of hysteresis associated with the introduction of Cu. When Cu is not intentionally added (Cu is well-known to be a naturally occurring trace impurity in CdTe for instance), we see little indication of hysteresis within our experimental error. This has been confirmed in every cell made in which Cu was intentionally absent. The presence of Cu introduces significant hysteresis in which  $W_d$  measured during the second (fwd) scan is always lower than the value of  $W_d$  determined during the first (rev) scan. Hysteresis in C-V measurements on polycrystalline thin film cells is also regularly reported by others [14, 15] in which the authors attribute this to the presence of deep states. The basis for this possibility is explained in more detail in [12].

Recently however, capacitance transients were used by Enzenroth, et al. [16] and Lyubomirsky, et al. [17] to determine the diffusion parameters of mobile  $Cu_i^+$  ions in CdTe and  $CuInSe_2$  cells and materials based upon a transient ion drift (TID) method first developed by Heiser and Mesli [18]. In particular, Enzenroth used the TID approach to quantify an increase in mobile  $Cu_i^+$  as a function of increased Cu added during cell fabrication. The presence of mobile charge, in particular,  $Cu_i^+$ , is thus plausible as an explanation for the effects shown in Fig. 5.

## II. EXPERIMENTAL DESIGN

Two sets of CdS/CdTe cells were fabricated in which the only difference between sets were the TCO/buffer structure used. In one set, a conventional bi-layer  $SnO_2$  structure consisting of undoped (insulating) and doped (conducting)  $SnO_2$ /Corning 7059 borosilicate glass superstrates were used to grow CdS/CdTe devices.  $SnO_2$  layers were grown by chemical vapor deposition (CVD) of tetramethyltin with bromotrifluoromethane ( $CBrF_3$ ) added when F-doping was required. Cells using these superstrate structures will be referred to as  $cSnO_2/iSnO_2$  cells. In the other set, cadmium (CTO) and zinc (ZTO) stannate materials were used as the conducting and buffer layer oxides. Stannate superstrate structures were fabricated by sputtering CTO and ZTO onto unheated borosilicate glass substrates with subsequent 650 °C anneals in He used to obtain the best optical and electrical properties. CdS and CdTe layers were deposited by chemical bath deposition (CBD) and close-spaced sublimation (CSS) respectively. Both sets used Cu-doped graphite prior to Ag paste metallization. Further details regarding the fabrication of cells can be found in references [1] and [19].

Performance data using standard J-V scans were made on cells after fabrication and during subsequent stress testing with a current-calibrated Oriel solar simulator. C-V measurements were performed in the dark at room temperature using an Agilent 4294A Precision Impedance Analyzer operated manually at 100 kHz with a 50 mV oscillation voltage. Capacitance data was collected by scanning voltage in two directions. Immediately upon applying a voltage of +0.5 V forward bias, capacitance was measured as voltage was quickly swept (~3 s) in a reverse (rev) direction to -1.5 V where bias was maintained for exactly 5 m. During the subsequent forward (fwd) sweep back to +0.5 V, capacitance data was again collected.

For stress testing, cells were placed glass-side up, under an Atlas CPS+ solar light source (~AM 1.5; 1-sun) in machined Al blocks designed to keep the cells at  $V_{oc}$  bias. Cell temperature was set at 100 °C. At times equal to 1, 4.4, 10, 28, 73, and 115 hrs cells were removed and allowed to relax in the dark for 12-24 hrs. After measurements of J-V and C-V, cells were again placed under stress. Some problems with temperature control were encountered during this test. It is very likely that actual stress temperatures exceeded 100 °C though the design of the Al blocks insured that all cells were at identical temperature.

## III. RESULTS AND DISCUSSION

The performance of cells, both initially as well as during stress testing are discussed in [12]. The uniformity of initial performance in cells grown on the  $SnO_2$ -based superstrates was very good. The highest performance achieved with this substrate was  $V_{oc} = 0.832$ ,  $J_{sc} = 23.2$ ,  $FF = 71.8$ , and  $\eta\% = 13.8$ . In contrast, considerable variation in performance was observed when using the CTO/ZTO superstrates. Some cells exhibited very high  $R_s$  due to cracking of the CTO/ZTO layers. However, the best performance ( $V_{oc} = 0.827$ ,  $J_{sc} = 24.6$ ,  $FF = 71.1$ ,  $\eta\% = 14.5$ ) was obtained using the CTO/ZTO substrate.

CTO/ZTO cell durability was also inferior to the  $\text{cSnO}_2/\text{iSnO}_2$  cells. This has been a somewhat consistent observation when testing CTO/ZTO cells fabricated at NREL. The durability of CTO/ZTO cells is determined however by both TCO and cell processing conditions and some discussion of this is presented in [12].

Of interest to this paper was the correlation observed between C-V hysteresis and cell performance during stress. Hysteresis is defined as the difference in  $W_d$  at  $V = 0$  between reverse and forward direction scans, i.e.,  $W_{d,rev} - W_{d,fwd}$ . Fig. 6 summarizes the variation of hysteresis with stress time as well as the correlation between  $V_{oc}$  and FF with hysteresis.

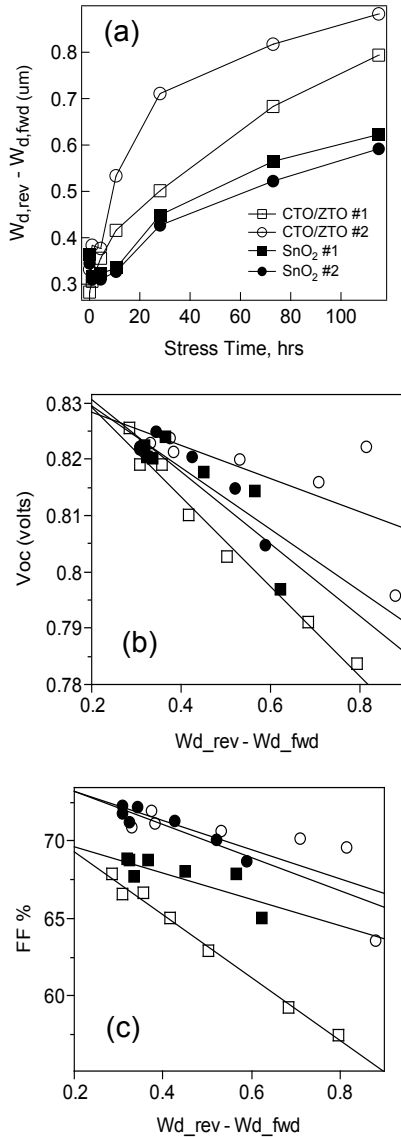


Fig. 6. Correlations during CdS/CdTe cell stress testing: (a) hysteresis vs. stress time, (b)  $V_{oc}$  vs. hysteresis, and (c) FF vs. hysteresis.

During stress, hysteresis was observed to increase as cell performance decreased. This increase with stress is shown in Fig. 6(a). The correlation of hysteresis with both  $V_{oc}$  and FF (shown in Fig. 6(b) and 6(c) respectively) was also apparent.

The correlation coefficient,  $R^2$  of  $V_{oc}$  with hysteresis for CTO/ZTO cells #1 and #2, and  $\text{SnO}_2$  cells #1 and #2 were 0.98, 0.46, 0.75, and 0.82. The same values for FF were 0.99, 0.58, 0.63, and 0.87. Similar correlations with either  $W_{d,fwd}$  or  $W_{d,rev}$  were not nearly as good and did not show the monotonic behavior shown in Fig. 6(b) and 6(c).

The origin of capacitance hysteresis during stress is not presently clear. Recent TID research suggesting an ionic basis is further supported by the early work by Snow, et al, who used hysteresis to measure ionic transport in insulating films [20]. In the context of this experiment, an ionic explanation would infer an important result. Since cells fabricated using the different TCO structures used identical Cu-doped back contacts, then the additional hysteresis shown in Fig. 6(a) for CTO/ZTO cells must be associated with the introduction of additional ions. In this case, the likely source would be from either the CTO or ZTO layers. C-V measurements are capable of detecting changes in charge below  $10^{15} \text{ cm}^{-3}$  and thus, this technique might be a useful way to measure ionic changes in the space-charge of cells in a non-destructive, and easily implementable way during stress testing. For example, the durability, in particular, chemical reactivity of new TCOs and buffers could be evaluated in such a fashion prior to costly scale-up of such structures in module manufacturing. Similarly, the effectiveness of various diffusion barriers to mitigate  $\text{Na}^+$  diffusion from soda-lime glasses might also be evaluated in such a fashion.

Regardless, an understanding of how best to interpret pre-bias dependent determinations of either  $W_{d,fwd}$  or  $W_{d,rev}$  are important since again, this is a key metric in understanding FF. The correlation of  $\eta\%$  with FF is extremely high for both initial performance as well as performance during stress testing.

#### IV. SUMMARY

An easy-to-implement, quick, and non-destructive technique was demonstrated for obtaining capacitance hysteresis measurements in thin-film polycrystalline solar cells. Initial results on CdS/CdTe solar cells stressed at approximately  $100^\circ\text{C}$  show a strong correlation between capacitance hysteresis (defined in this study as the difference in depletion width at  $V=0$ ) with cell  $V_{oc}$  and FF was shown. The origin of this hysteresis, whether electronic or ionic, is unclear though past work suggests an ionic nature. The technique shows potential for being an important diagnostic tool for understanding why FF in these cells change with stress.

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<b>14. ABSTRACT (Maximum 200 Words)</b> In this paper we present the correlation of CdTe solar cell performance with capacitance-voltage hysteresis, defined presently as the difference in capacitance measured at zero-volt bias when collecting such data with different pre-measurement bias conditions. These correlations were obtained on CdTe cells stressed under conditions of 1-sun illumination, open-circuit bias, and an acceleration temperature of approximately 100°C.						
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