Publications (E)   Energy

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Presented at the Reliability of Photovoltaic Cells, Modules, Components, and Systems III: SPIE Conference
San Diego, California
August 3-5, 2010

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Effect of Hysteresis on Measurements of Thin-Film Cell Performance

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ABSTRACT

Transient or hysteresis effects in polycrystalline thin film CdS/CdTe cells are a function of pre-measurement voltage bias and whether Cu is introduced as an intentional dopant during back contact fabrication. When Cu is added, the current-density (J) vs. voltage (V) measurements performed in a reverse-to-forward voltage direction will yield higher open-circuit voltage (V_{oc}), up to 10 mV, and smaller short-circuit current density (J_{sc}), by up to 2 mA/cm^2, relative to scanning voltage in a forward-to-reverse direction. The variation at the maximum power point, P_{max}, is however small. The resulting variation in FF can be as large as 3%. When Cu is not added, hysteresis in both V_{oc} and J_{sc} is negligible however P_{max} hysteresis is considerably greater. This behavior corroborates observed changes in depletion width, W_d, derived from capacitance (C) vs voltage (V) scans. Measured values of W_d are always smaller in reverse-to-forward voltage scans, and conversely, larger in the forward-to-reverse voltage direction. Transient ion drift (TID) measurements performed on Cu-containing cells do not show ionic behavior suggesting that capacitance transients are more likely due to electronic capture-emission processes. J-V curve simulation using Pspice shows that increased transient capacitance during light-soak stress at 100 °C correlates with increased space-charge recombination. Voltage-dependent collection however was not observed to increase with stress in these cells.

Keywords: CdTe solar cell, transient capacitance, DLTS, transient ion drift, reliability, degradation, voltage-dependent collection

1. INTRODUCTION

Transient and metastable effects in polycrystalline thin film modules significantly affect module performance measurements. Storage conditions concerning light-exposure, bias, and temperature can change not only power, but also measurements of open-circuit voltage (V_{oc}), short-circuit current-density (J_{sc}), and fill-factor (FF) [1]. The magnitude of these effects is observed to vary as modules undergo accelerated lifetime testing [2]. Uncertainty regarding pre-measurement conditions during module shipment and storage and the resulting effect on performance justifies the need for stabilization procedures prior to module performance measurements during qualification and field-test studies.

Recent research has concentrated on studying the nature of transients in capacitance-voltage (C-V) measurements applied to small-area CdTe devices [3] as well as production-sized CdTe and Cu(In,Ga)Se$_2$ modules [2]. These studies involve measuring the capacitance as a function of sequential forward-to-reverse (termed a "rev" direction) and reverse-to-forward (termed a "fwd direction) voltage scans with a 5 m hold at reverse-bias. In [3], CdS/CdTe devices were fabricated on two, uniquely different transparent conducting oxides (TCOs) in which the durability of the device under 1-sun, V_{oc} bias, 100 °C stress testing was notably affected by the TCO type. The rate of degradation observed in CdS/CdTe devices fabricated on insulating zinc-stannate (ZTO)/cadmium stannate (CTO) TCO/Corning 7059 borosilicate glass substrates was in general, greater relative to identically fabricated CdS/CdTe devices fabricated on more traditional, undoped, insulating tin-oxide (iSnO$_2$)/F-doped conductive tin-oxide (cSnO$_2$) TCO/borosilicate glass substrates. Depletion width (W_d = [ε·A]/C where ε is the dielectric permittivity, A is the cell area) hysteresis (defined as the difference in W_d measured at V=0 between fwd and rev voltage scans) was observed to correlate strongly with performance during stress testing. The variation in W_d hysteresis with stress time as well as the correlation of this capacitance-derived measurement with both V_{oc} and FF measured during stress is shown in Figure 1. The increased hysteresis seen in Fig. 1(a) paralleled decreased performance during stress. The reasonably good correlation of hysteresis with both V_{oc} and FF (shown in Fig. 1(b) and 1(c) respectively) is also apparent.

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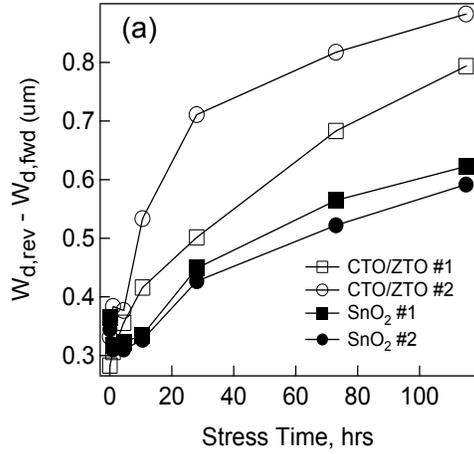
Figure 1. Variation of C-V hysteresis with stress time (a) for CdS/CdTe devices deposited on either CTO/ZTO or SnO$_2$-based TCO/glass substrates and subsequent correlations of (b) V$_{oc}$ and (c) FF with hysteresis. Hysteresis is defined as the difference in W$_d$ measured at V = 0 between rev and fwd voltage scans.
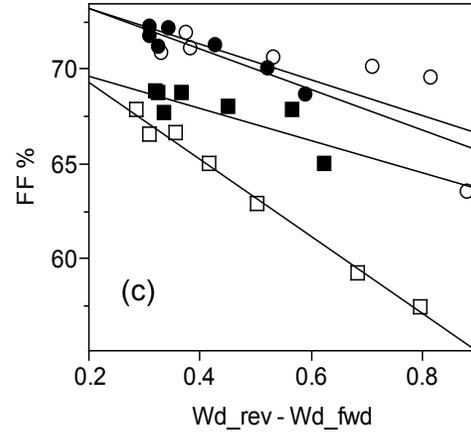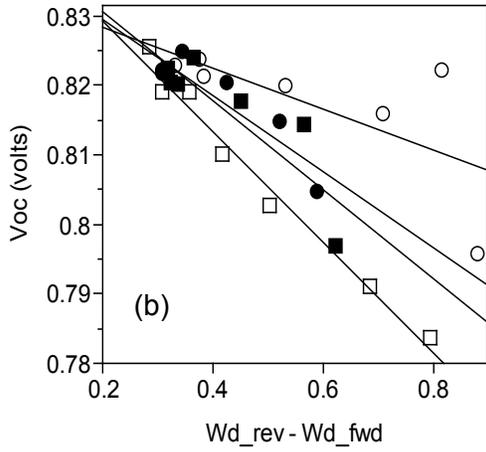
The linear correlation coefficient, R^2, of V$_{oc}$ with hysteresis for CTO/ZTO cells #1 and #2, and SnO$_2$ cells #1 and #2, were 0.98, 0.46, 0.75, and 0.82, respectively. Similar correlations for FF were 0.99, 0.58, 0.63, and 0.87 respectively. When analyzed without considering hysteresis, i.e., based on either W$_{d,fwd}$ or W$_{d,rev}$ separately, correlations were not nearly as high and tended to show non-monotonic behavior.

The origin of this capacitance hysteresis was not substantiated. From an electronic perspective, hysteresis could be explained by considering majority carrier trap emission within the CdTe space-charge region. Depletion widths measured during a rev-voltage scan will initially be higher since the negative space-charge (i.e., N$_a^-$) region of the CdTe is screened by holes occupying deep states in the band gap. At a fixed reverse bias (1.5 V in [3]), some deep states fall below the Fermi level and the resulting, time-dependent hole emission (or electron capture) will reduce this screening causing W$_d$ to decrease. The subsequent fwd-direction voltage scan (-1.5 V to +0.2 V) captures this reduced value of W$_d$ such that hysteresis, W$_{d,rev}$–W$_{d,fwd}$ is positive. This filling and emptying of deep states gives rise to capacitance transients which are fundamental to deep level transient spectroscopy (DLTS) measurements. Based upon this model, hysteresis is proportional to the density of deep states within the CdTe space-charge undergoing capture-emission processes, and an increase in hysteresis would represent an increase in electronic traps with stress.

Another mechanism for hysteresis, based upon transient ion drift (TID) was also presented. This seemed plausible given the previous reports of TID behavior in both polycrystalline CdTe [4] and CuInSe$_2$ [5] devices which themselves were based upon earlier works by Heiser and Mesli [6] and subsequently, Lyubomirsky, et al. [7]. In the TID model for hysteresis, the higher W$_d$ measured during the rev-voltage scan is due to the screening of the space-charge region, not by holes, but rather by positively charged Cu-interstitial donors, Cu$_i^+$. Again, at a fixed reverse bias of 1.5 V, these donors are attracted toward the back contact, away from the space-charge, with the same net effect, i.e., a decrease in W$_d$ again

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due to reduced screening. However, according to Heiser and Mesli, the transients observed in TID are distinguishable from those in TID. Referring to the capacitance change occurring at reverse and positive bias as accumulation (Cu_i^+ accumulating towards the back contact) and flattening (Cu_i^+ re-distribution towards the space-charge) processes respectively, they note that relaxation times at reverse and forward bias levels, τ_a and τ_f, should follow the relationship $\tau_f / \tau_a > 1$ and be reverse bias dependent, that is, the ratio should increase with increasing reverse-bias. This was argued as not the case for DLTS processes where the capture rate is much higher than the emission rate, and generally independent of reverse bias. The C-V technique described in [3] unfortunately did not record decay rates at either +0.2 or -1.5 V. It was stated however, that there was no obvious mechanism by which an increase in mobile ions (as explanation for the increased hysteresis shown in Fig. 1) would degrade performance, but rather, the formation of deep states and possibly increased recombination that would most likely decrease performance during stress testing.

This paper reports on a modification of the C-V technique used in [3] such that capacitance response is measured during the initial reverse-bias pulse (τ_a) and a subsequent, relaxation bias at V=0 (τ_f). By repeating this measurement at progressively increasing reverse-bias levels, the voltage-dependence of the term τ_f / τ_a can be determined. The effect of the strong variation in W_d with voltage-scan direction shown in Fig. 1(a) on the J-V characteristics of cells with and without Cu as an intentional dopant is also shown. Finally, further insight regarding the mechanism of degradation reported in [3] is ascertained using PSpice modeling of device J-V characteristics measured during stress.

2. EXPERIMENTAL PROCEDURE

Cell Fabrication

The structure and fabrication history of CdS/CdTe cells used in this study is discussed in reference [3]. The basic structure is that of a Corning 7059 borosilicate glass superstrate design in which light passes through a glass/TCO/buffer construction (either $7059/cSnO_2/iSnO_2$ or $7059/CTO/ZTO$), where it is then absorbed in the n-(CdS)/p-(CdTe) heterojunction. A schematic of the different layers comprising the device is shown in Fig. 2.
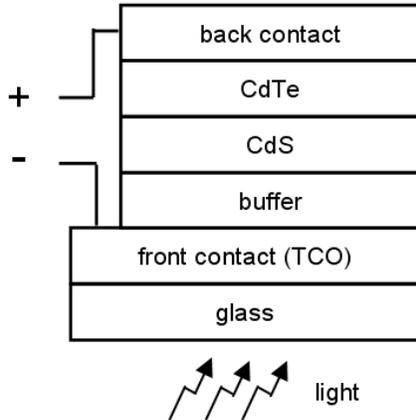
Figure 2. CdS/CdTe device superstrate structure. The TCO layer is either CTO or $nSnO_2$ while the corresponding buffer is either ZTO or $iSnO_2$.

The CTO/ZTO and SnO_2-based TCOs were deposited by sputtering and low-pressure, chemical vapor deposition. The $cSnO_2$ and $iSnO_2$ layers were deposited onto bare glass substrates heated to 550 ℃ using tetramethyltin, bromotrifluoromethane ($CBrF_3$), and oxygen. The $CBrF_3$ provides the fluorine dopant for the $cSnO_2$ layer alone. The $cSnO_2$ and $iSnO_2$ layers were 500 and 100 nm thick respectively. The resulting sheet resistance of this bi-layer stack measures ~ 9 Ω /sq. The CTO and ZTO layers were sputtered onto unheated substrates to a thickness of 320 and 150 nm respectively. After each sputter deposition, the amorphous oxide layers were annealed in 30 Torr He for 15 min at 650 ℃ with the oxide film in contact with a CdS film/Corning 7059 glass plate (i.e., a "close-proximity" anneal). During the subsequent anneal, the optical band gap of the CTO layer increases from about 3.0 eV to 3.5 eV with a several order

magnitude drop in resistivity to ~1.8 x 10^{-4} Ω·cm. The CTO layer exhibits some crystallization during this post-deposition anneal. The iSnO$_2$ and ZTO buffer layers (after anneal) are insulating with a resistivity of around 1-10 Ω·cm and contribute little additional absorption loss to the oxide layer stack. The CdS layer is grown by chemical bath deposition at ~90 °C to a thickness of approximately 80 nm. The CdTe layer is deposited onto the CdS/buffer/TCO/glass substrate in a close-spaced sublimation (CSS) arrangement where the CdTe source and substrate temperatures are 660 and 625 °C respectively. An ambient of 15 torr He and 1 torr O$_2$ is used during CSS. After the CdTe deposition, the CdTe/CdS/buffer/TCO/glass structure was then exposed to vapor CdCl$_2$ treatments in an oxygen/helium ambient (100 Torr O$_2$ + 400 Torr He). Prior to the back contact application, CdTe surfaces were etched in a nitric-phosphoric acid solution in order to form a beneficial, Te-rich layer and to remove surface oxides [8]. Back contacts concluded with the application of a relatively thick layer (~50–100 μm) of graphite paste containing Cu$_x$Te and HgTe dopants followed by a similarly thick, final conducting layer of Ag paste. Cells without intentional Cu dopant use only the graphite paste. A narrow (~1 mm) margin of CdTe surrounding the perimeter of the dopant/Ag paste contact was used to reduce edge shunting.

J-V and C-V Measurements

Performance data using standard current versus voltage (J-V) scans were made on cells after fabrication (t = 0) and during stress testing (t > 0) with a current-calibrated Oriel solar simulator. In an attempt to average out J-V transients due to pre-bias and voltage scan directions, the voltage applied across the probes is routinely swept continuously from a fwd-bias to rev-bias in a saw-tooth fashion while Kelvin probes are lowered onto the front and back contacts of the device. With probes attached, and after the next subsequent voltage sweep, current as a function of voltage is collected first in the dark from fwd to rev-bias. The simulator shutter is then opened, exposing the cell to a pre-calibrated 1-sun irradiance spectrum with the photocurrent measured during the subsequent fwd to rev-scan. In this fashion, transients are managed and repeatable measurements of performance are obtained for monitoring relative degradation during stress testing. A small indium pad is placed between the back contact and Kelvin probe to minimize potential damage to the cell by the sharp probe tips. To ascertain what effect the hysteresis in depletion width shown in Fig. 1(a) has on cell performance, this voltage sweeping technique was not used. Rather, cells were first biased at -1.5 V for 5 m in the dark, at which point the current was measured as the voltage was swept from -1.5 V to +0.2 V. At +0.2 V, the cell was then placed in the dark for an additional 5 m, and the light photocurrent was measured as the voltage was scanned from +0.2 V to -1.5 V.

Capacitance-voltage (C-V) measurements (dark at room temperature) were performed using an Agilent 4294A Precision Impedance Analyzer operated at 100 kHz with a 50 mV oscillation voltage. The capacitance is relatively insensitive to frequency at 100 kHz. Unlike in [3], a Labview program was used to automate data collection to insure repeatability. The same bi-directional voltage scan used in [3] was replicated except that three successive loops in voltage between V=0 and increasing reverse biases of -1.0, -2.0, and -3.0 V were performed with capacitance transient data collected at the termination of each voltage scan. After some experimentation, a pause time of 20 m was used to collect transient data at each terminating voltage. This is twice as long as the collection time used in reference [4] and was determined to be adequate for obtaining linear fits of ln [ΔC] functions with time for calculating relaxation time constants. The relaxation time constants for τ_a and τ_f were determined respectively, using the following relationships:

$$\frac{C(\infty) - C(t)}{C(\infty) - C(0)} = \exp\left(- t/\tau_a\right) \qquad (1)$$

$$\frac{C(t) - C(\infty)}{C(0) - C(\infty)} = \exp\left(- t/\tau_f\right) \qquad (2)$$

where C(t), C(0), and C(oo) equal the capacitance as a function of time, as well as the capacitance at the beginning and end of each 20 m transient measurement period. The resulting capacitance change with time for a representative Cu-containing cell is shown in Fig. 3.
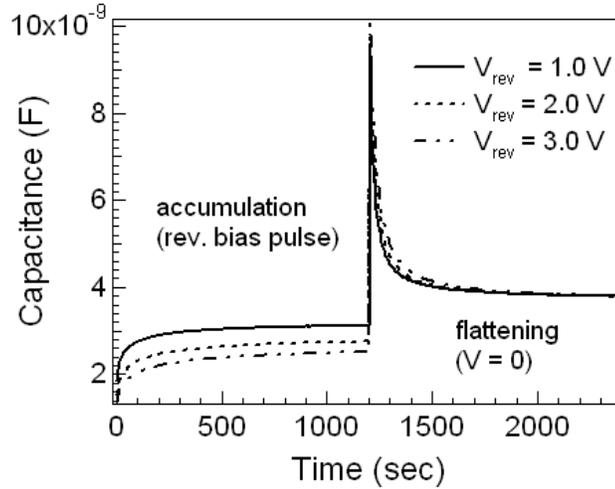
Figure 3. Capacitance versus time for a three cycle loop with progressively increasing rev-bias voltage.

The increasing capacitance during the accumulation period, where the cell is subjected to a reverse bias pulse, corresponds to a value for W_d which decreases with time (C increases). C(0) and C(oo) in equation (1) correspond to the capacitance measured at t = 0 and 1200 s (20 m). The voltage is then swept to V = 0 capturing the hysteresis discussed in [3]. The voltage is maintained at this level for an additional 20 m where W_d increases (C decreases). C(0) and C(oo) in equation (2) corresponds to the capacitance measured at t=1200$^+$ and 2400 s.

Accelerated lifetime test (ALT) conditions have been described before [3]. In brief, cells were placed, glass-side up, under an Atlas CPS+ solar light source (~AM 1.5; 1-sun) in machined Al blocks designed to keep cells at V_{oc} bias. Cell temperature was set to 100 ºC. At times equal to 1, 4.4, 10, 28, 73, and 115 hrs, cells were removed and allowed to stabilize in the dark for 12-24 hrs. After measurements of J-V and C-V, cells were again placed under stress. Sometime after the last measurement at t=115 hrs, the temperature controllers failed (over a weekend) resulting in excessive heating and destruction of cells. The actual test temperature of 100 ºC is suspect (temperatures may have been higher) particularly near the conclusion of the test. Regardless, the design of the Al blocks at least assures us that cells were tested at the same temperature.

J-V Curve Modeling

PSpice simulations provide a near-quantitative method for determining losses in devices as a function of stress. In Fig. 4, a parallel combination of forward-biased diodes is used to independently simulate recombination currents in the quasi-neutral (J_{QNR}) and space-charge (J_{SCR}) regions. Back contact behavior is represented by a parallel combination of a reverse-biased diode (represented by the leakage current J_b) and a shunt conductance ($1/R_b$) that was previously used to model the J-V characteristics of contacts commonly observed in 1st quadrant J-V behavior [9]. The theoretical basis for the two-diode model as a general expression for the current produced in a solar cell can be found in reference [10].
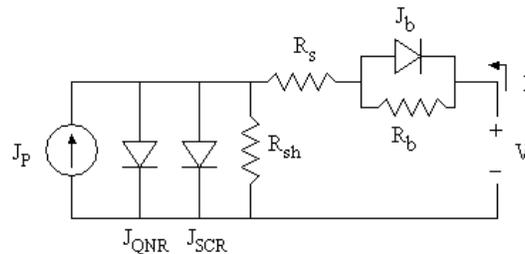
Figure 4. Two-diode solar cell discrete element circuit model.

Losses associated with any of the circuit elements shown in Fig. 4 can be determined by comparing J-V curves before and after some change in the cell. For example, Fig. 5 demonstrates a nearly exact fit for a 14.4% cell in which the following parameters were determined: J_p = 0.024409 A/cm^2, J_{01} = 0.5e^{-16} A/cm^2, J_{02} = 2e^{-09} A/cm^2, R_s = 1.9 ohm*cm^2, R_{sh} = 200k ohm*cm^2, J_b = 6e^{-02} A/cm^2, and R_b = 1.5 ohm*cm^2. The "loss" associated with this cell, relative to a theoretical, maximum performance cell can be determined by generating the latter J-V curve as shown in Fig. 5 in which J_{01} and J_{02} are both set to ideal values of 1e^{-20}, $R_s \rightarrow$ 0, $R_{sh} \rightarrow$ oo, and J_b and R_b are removed from the model. The corresponding ideal cell has J-V parameters of V_{oc} ~ 1.095 V, J_{sc} ~ 24.4 mA/cm^2, FF ~ 89.0, and efficiency of ~23.8% suggesting the performance entitlement of this technology if processing induced "losses", in particular those resulting in high recombination currents can be eliminated. This approach has recently been used to explain general degradation mechanisms in CdS/CdTe devices as a function of stress [11].
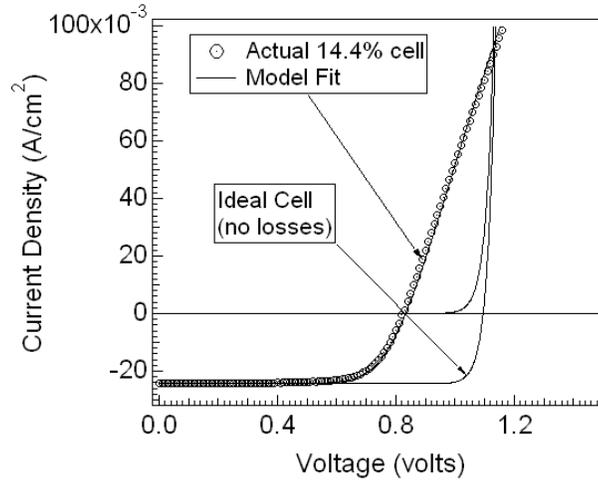

Figure 5. PSpice simulation of a high-efficiency CdS/CdTe device and the potential improvement in J-V behavior if all losses are removed (ideal cell).

A major weakness of PSpice, however, is its inability to adequately determine voltage-dependent collection losses since J_p in the PSpice model is constant, and not a function of voltage. Thus, superposition is guaranteed. The high degree of superposition between the light and dark J-V curves for the ideal cell shown in Fig. 5 was obtained simply by setting J_p=0 in the dark J-V simulation. In general, polycrystalline thin film solar cells do not demonstrate this degree of superposition [12]. However, as discussed in reference [11], the differences between actual J-V data and the PSpice simulations can be used to determine this voltage-dependent photocurrent loss. The value of J_p is set to the current measured at the greatest value of reverse-bias. R_s is then determined by dV/dJ in the first quadrant. As long as roll-over is not extreme (J_b approaching zero), this value can be determined. R_{sh} is subsequently determined by using the value of dV/dJ at V=0 from the dark J-V curve since there is nothing to suggest a photo-active shunt conductance. The remaining parameters J_{QNR} and J_{SCR} are then adjusted to fit V_{oc}. When performed in this manner, the actual J-V photocurrent will generally be lower than the simulated value since the latter again assumes a constant value of J_p. The difference between these two curves represents the voltage-dependent loss.

3. RESULTS AND DISCUSSION

Pre-bias Effects on Cell Performance

Fig. 6 shows how pre-biasing the cell at either 1.5 V reverse bias and 0.2 V forward bias can affect the J-V characteristics of cells with and without intentional Cu added as a dopant to the graphite paste contact described previously. The behavior shown in Fig. 6 is representative of the 16 cells (8 each with and without Cu) fabricated for this measurement.

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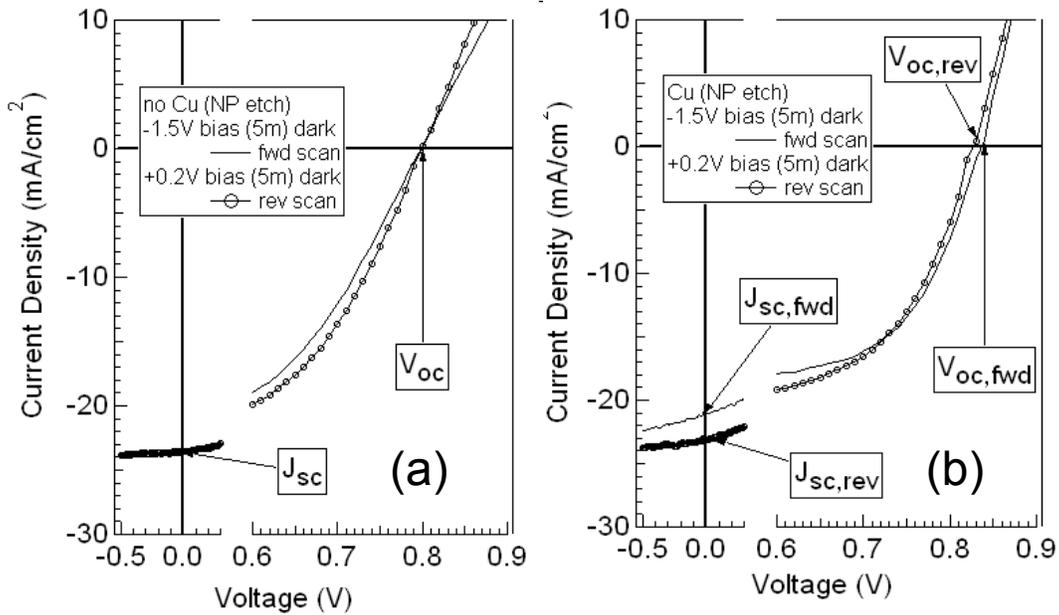
Figure 6. Representative variation in cell J-V curve behavior based upon pre-measurement bias and sweep direction for CdS/CdTe cells without (a) and with (b) intentional Cu added as a dopant.

V_{oc} and J_{sc} were strongly impacted by pre-measurement bias and sweep direction only for devices that contained Cu. At the same time, the behavior at P_{max} (where J-V curves cross) was significantly less. Scanning the cell in a fwd direction from an initial reverse bias — where C-V data would suggest a smaller W_d — caused a strong reduction in J_{sc} (1-2 mA/cm^2) and increase in V_{oc} (5-10 mV). The net effect on FF is an increase of 1-3% points. This is similar to the increase in FF observed in testing CdTe modules when tracing current-voltage from V=0 (I_{sc}) to V_{oc} (see for example Fig. 5 in reference [1]). This overall behavior is consistent in devices where voltage-dependent collection limits performance. V_{oc} and J_{sc} transients for cells not containing Cu were negligible, though a slight J-V curve hysteresis near P_{max} was observed. FF was slightly less in cells not containing Cu when scanning voltage in the fwd direction. It should be noted that the distinction between cells "containing" and "not containing" Cu refers only to whether Cu was *intentionally* added during back contact processing. Cu may exist as a trace impurity in cells not intentionally doped with Cu, and thus the reason for the very slight hysteresis observed here in J-V measurements and in the C-V data presented earlier in [3].

TID measurements

Using the C-V technique described earlier to collect capacitance transient response at V=0 and progressively increasing values of reverse bias, equations (1) and (2) were employed to determine relaxation time constants in cells containing Cu. Capacitance transients in cells without Cu are too small to differentiate from noise in such measurements. Shown in Fig. 7 are the ln (ΔC) functions plotted as a function of time and the corresponding relaxation time constants for accumulation (τ_a) occurring during the reverse-bias pulse (7(a)) and flattening (τ_f) at V = 0 (7(b)) for each of the three reverse-bias voltage levels studied. The latter values were determined from the inverse slope of the curves between t= 200 and 800 s. These measurements were performed for several cells containing Cu. The example shown here is representative of the overall behavior and will be used for this discussion. The ratio τ_f / τ_a with increasing reverse bias is shown to equal 0.85, 0.79, and 0.72 in this case. This behavior does not meet either of the two primary criteria for identifying ionic drift as discussed previously. Thus, at this point, it does not appear that the hysteresis observed in these cells has an ionic basis though this work is somewhat preliminary. For example, frequency domain measurements might be used to selectively freeze out ionic processes.
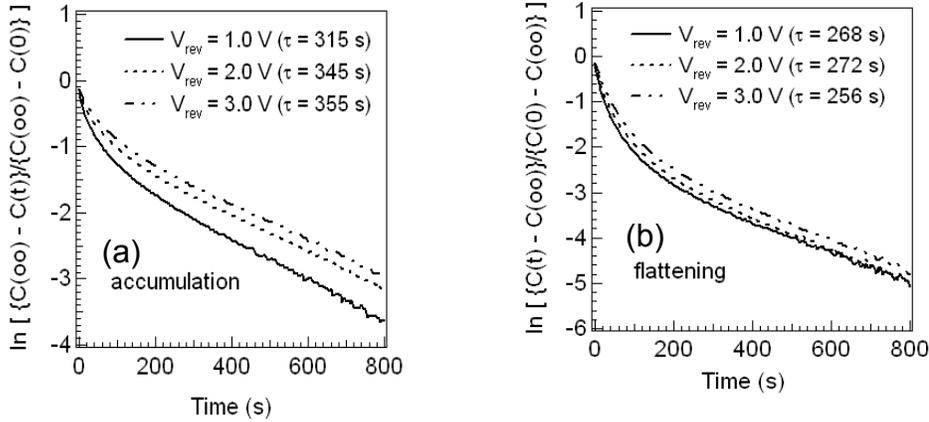
Figure 7. Transient capacitance response during the accumulation (a) and flattening (b) processes occurring at reverse-bias and V=0 conditions respectively.

J-V Curve Modeling

J-V curves corresponding to cells CTO/ZTO #1 and SnO$_2$ #1 from Fig. 1 at t = 0 and t = 115 hrs were fit using the PSpice technique described previously. Actual and simulated J-V data for the CTO/ZTO and SnO$_2$ cells are shown in Fig. 8(a) and 8(b) respectively. The current density axis has been adjusted to magnify the difference observed between simulated and actual photocurrents. The difference between actual and fit graphs represent the additional current loss not determined by the discrete element model of Fig. 4. In each case, R$_{sh}$ was determined by the behavior of the dark J-V curve at V = 0 (not shown).
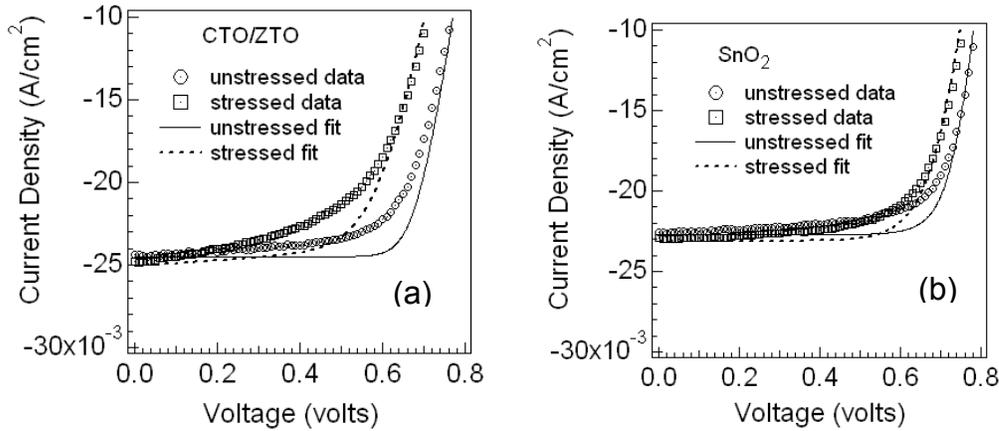
Figure 8. Comparison of actual J-V data and PSpice simulated data for unstressed (t=0) and stressed (t=115 hrs) CTO/ZTO-based (a) and SnO$_2$-based (b) cells.

The circuit model fit parameters for the simulated J-V curves are summarized in Table 1. Times are given in hrs, current density is expressed in A/cm^2, and resistive terms given in $\Omega \cdot$cm^2. The primary reason for the greater rate of degradation in the CTO/ZTO cells appears to be due to both increased shunting (lower R$_{sh}$), and increased space-charge recombination. At the same time, voltage-dependent collection does not appear to increase significantly with stress for CdTe devices using either substrate type. Increased recombination is likely due to the increased deep state density during stress testing. The latter manifests as an increase in the capacitance hysteresis observed during stress. It is interesting to note that the increased concentration of deep states does not appear to significantly increase voltage-dependent collection.

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Substrate	Stress Time	Jp	J(o1)	J(o2)	Rs	Rsh	Rb	Jb
CTO/ZTO	0	0.024502	3.00E-16	8.00E-10	4.3	200K	0.5	1.00E-01
CTO/ZTO	115	0.025289	3.00E-16	5.70E-09	4.6	595	6.7	2.70E-02
iSnO2/SnO2	0	0.02273	2.50E-16	6.00E-10	2.4	200K	1.3	8.50E-02
iSnO2/SnO2	115	0.023104	2.50E-16	2.90E-09	2.6	200K	4.6	4.80E-02

Table 1. PSpice Fit parameters of initial and degraded J-V performance for CdTe devices deposited on both CTO/ZTO and iSnO$_2$/SnO$_2$ substrates

4. CONCLUSIONS

The transient behavior observed in C-V measurements obtained on CdTe devices deposited on either SnO$_2$ or CTO/ZTO based substrates is likely due to the presence of deep states in the space-charge region. The increase in C-V hysteresis with stress testing of these cells is likely due to an increase in deep state density. This increases space-charge recombination. Higher levels of hysteresis are correlated with higher levels of degradation in cells. The latter is correlated with higher levels of recombination. Increased recombination does not appear to increase voltage-dependent collection. TID measurements performed as part of our C-V measurement technique do not support the motion of ions for explaining hysteresis. Again, the latter is more reflective of an increase in the density of deep states.

5. ACKNOWLEDGEMENTS

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REPORT DOCUMENTATION PAGE

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1. REPORT DATE *(DD-MM-YYYY)* March 2011	2. REPORT TYPE Conference Paper	3. DATES COVERED *(From - To)*

4. TITLE AND SUBTITLE Effect of Hysteresis on Measurements of Thin-Film Cell Performance	5a. CONTRACT NUMBER DE-AC36-08GO28308
	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S) D. Albin and J. del Cueto	5d. PROJECT NUMBER NREL/CP-5200-48996
	5e. TASK NUMBER PVA9.2450
	5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393	8. PERFORMING ORGANIZATION REPORT NUMBER NREL/CP-5200-48996

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S) NREL
	11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words)*
Transient or hysteresis effects in polycrystalline thin film CdS/CdTe cells are a function of pre-measurement voltage bias and whether Cu is introduced as an intentional dopant during back contact fabrication. When Cu is added, the current-density (J) vs. voltage (V) measurements performed in a reverse-to-forward voltage direction will yield higher open-circuit voltage (Voc), up to 10 mV, and smaller short-circuit current density (Jsc), by up to 2 mA/cm2, relative to scanning voltage in a forward-to-reverse direction. The variation at the maximum power point, Pmax, is however small. The resulting variation in FF can be as large as 3%. When Cu is not added, hysteresis in both Voc and Jsc is negligible however Pmax hysteresis is considerably greater. This behavior corroborates observed changes in depletion width, Wd, derived from capacitance (C) vs voltage (V) scans. Measured values of Wd are always smaller in reverse-to-forward voltage scans, and conversely, larger in the forward-to-reverse voltage direction. Transient ion drift (TID) measurements performed on Cu-containing cells do not show ionic behavior suggesting that capacitance transients are more likely due to electronic capture-emission processes. J-V curve simulation using Pspice shows that increased transient capacitance during light-soak stress at 100 ºC correlates with increased space-charge recombination. Voltage-dependent collection however was not observed to increase with stress in these cells.

15. SUBJECT TERMS
CdTe solar cell; transient capacitance; DLTS; transient ion drift; reliability; degradation; voltage-dependent collection

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified	UL		19b. TELEPHONE NUMBER *(Include area code)*

F1147-E(10/2008)