Analysis and design of low power CMOS ultra wideband receiver

Abdul Bhuiyan
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ANALYSIS AND DESIGN OF LOW POWER CMOS ULTRA WIDEBAND RECEIVER

by

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ABSTRACT

Analysis and Design of Low Power CMOS Ultra Wideband Receiver

by

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University of Nevada, Las Vegas, 2009

This research concentrates on the design and analysis of low power ultra wideband receivers for Multiband Orthogonal Frequency Division Multiplexing systems. Low power design entails different performance tradeoffs, which are analyzed. Relationship among power consumption, achievable noise figure and linearity performance including distortion products (cross-modulation, inter-modulation and harmonic distortion) are derived. From these relationships, circuit design proceeds with allocation of gain among different sub circuit blocks for power optimum system.

A power optimum RF receiver front-end for MB-OFDM based UWB systems is designed that covers all the MB-OFDM spectrum between 3.1 GHZ to 9.6 GHZ. The receiver consists of a low-noise amplifier, down-converter, channel select filter and programmable gain amplifier and occupies only 1mm$^2$ in 0.13um CMOS process. Receiver consumes 20 mA from a 1.2 V supply and has the measured gain of 69db, noise figure less than 6 dB and input IIP$_3$ of -6 dBm.
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CHAPTER 1

INTRODUCTION

1.1 Motivation

Wireless connectivity products in both home and office are playing a significant role in today’s communication system. The most popular communication gadgets include black-berry, cellular telephone and wireless local area network (WLAN) peripherals, etc. Wireless connectivity products mentioned above strive to provide information access “at any place any time” but at low data rate. Consumer demand for higher data is increasing as the popularity of wireless connectivity products increases. Wireless networks beyond 3G would make higher data rate connectivity possible in near future. The phenomenal development in wireless technology in recent years would usher in a new era of ubiquitous network enabling “everybody and everything at any place any time”.

Current dominant wireless network technology include wireless wide area network (WWAN), wireless local are network (WLAN) and wireless personal area network (WPAN). WWAN network can support data rate up to few million bits per second (MBPS) for a several mile wide area via both terrestrial and satellite links. Wimax is a promising WWAN technology that can provide high data rate communication. However, high power consumption and high installation cost are the major impediments to WWAN.
WLAN, which gained tremendous popularity in broadband internet connection in recent years, has the potential to provide raw data rate up to 54 MBPS. The most popular WLAN solution Wifi (IEEE 802.11 a/b/g) gained tremendous commercial success but its use is limited in low power applications. Similar to WWAN, WLAN is very power hungry as the network is designed for relatively long range (over 100 ft) [2].

WPAN, on the other hand, tend to be low power as the network coverage is reduced to only a few feet. Dominant WPAN technologies include Infrared-communication, Bluetooth and Zigbee [3]. Infrared communication can support low data rate in line of sight communication while Bluetooth and Zigbee can offer raw data rate of 3 MBPS and 1 MPBS respectively in non line of sight communication. However, data rates of these technologies are significantly short of the rates needed for the following applications in short range communication [4]:

1. High-speed cable replacement, including downloading pictures from digital cameras to PCs and wireless connections between DVD players and projectors.

2. Wireless replacement for Universal Service Bus (USB) connections for computers and peripherals in home and office environments.

3. Wireless video projectors and home entertainment systems with wireless connections between components.

4. Coexistence and networking of audio, still video, and motion pictures for fixed and portable low-power devices.

5. Home network of audio and video with internet gateway.
6. Multimedia wireless distribution system for dense user environments, such as multi-tenant units/multi-dwelling units.

7. Office, home, auto, and wearable wireless peripheral devices.

As these applications would require data rate in the range of several hundred MBPS, interest in ultra-wideband (UWB) grew since UWB based system can meet the demand of high data rate in a power and cost efficient manner. Furthermore, UWB offers greater immunity against multipath environment and in-band jammers, making it attractive for high data rate indoor communication.

UWB band spans a very large unlicensed spectrum (7.5 GHZ) from 3.1 – 10.6 GHZ, with an average power level of only -41.3 dBm / MHZ [5]. Although UWB standard has not yet been adopted, three competing physical layer (PHY) standards are proposed. First is the direct sequence ultra-wideband (DS-UWB) system, second is the multi-band orthogonal frequency division multiplexing (MB OFDM – UWB) and third is impulse radio based system (IR-UWB). The DS-UWB system transmits short duration pulses with position or polarity modulation spreading signal bandwidth to few gigahertz. The MB-OFDM UWB system subdivides the entire 7.5 GHZ bandwidth to fourteen 528-MHZ sub-bands and performs orthogonal frequency division multiplexing (OFDM) within each sub-bands and frequency hopping among the sub-bands. IR-UWB transmits short duration pulses without using any carrier. Chapter 2 provides further details on UWB.

Numerous technological challenges, which include efficient modulation, coding techniques, wideband RF circuits and baseband ADC, continue to plagues widespread adoption of UWB technology. The most challenging component at UWB PHY level is
RF front ends (antenna, low noise amplifiers, power amplifiers and frequency synthesizer) since these circuit components need to perform in a broad range of frequency spectrum while consuming very little power and with little area overhead. Traditional design methodology practiced in the era of narrow band can’t meet the challenges of broadband system, thus new circuit topologies and design methodologies are needed.

1.2 Research Goals

The goal of this research is to identify the design tradeoffs and develop design methodology for RF front-ends for MB-OFDM UWB systems that operates in 3.1 - 10.6GHz bands.

Design flow follows a top-down approach: starting at the system level specification and deriving specifications for the RF front-end circuits while taking realistic antenna and baseband specification in cognizance. Finding a global optimum design can be endless procedure since many of the RF front-end circuit’s power optimum performance is cross-dependent. Therefore, design methodology involves finding power optimum design within the assigned power budget while maintaining overall system performance specifications. Furthermore, design methodology would be geared toward submicron RF CMOS process, which is the technology of choice for low cost system. As low cost system would also require elimination of both on and off chip passive components, research would investigate design challenges in such low cost semiconductor process. The research follows the steps as shown below:

1. Evaluate design tradeoffs for MB-OFDM UWB receiver RF front-end circuits.
2. Find a methodology for the design of power optimum RF front-end circuits in submicron RF CMOS submicron process.

3. Identify performance trade-offs in elimination of on and off chip inductors in RF-front end circuits.

4. Design the front-end circuits to prove the validity of circuit design methodology developed while meeting the overall system specifications.

1.3 Thesis Organization

Chapter 2 discusses fundamentals of wireless communication, propagation loss, fading, receiver architectures, sensitivity linearity, and etcetera. These receiver attributes are important for understanding communication system design presented in later chapters. Chapter 3 gives a basic UWB communication background, such as data rate and modulation scheme and an overview of OFDM and MB OFDM, which offers greater flexibility in UWB system implementation.

Chapter 4 develops design methodology for low power MB OFDM UWB receiver and highlights design trade-offs such as noise figure, linearity and distortion. Accuracy of design theories developed is verified with the result of full system simulation. Chapter 5 presents the CMOS technology used in this project and insights to transistor modeling. Additionally, chapter discusses inductor and capacitor physical implementation in CMOS and modeling parameters.

Chapter 6 focuses on different RF circuit blocks and performance tradeoffs involved in designing low power and low cost design. Low cost implementation strives to eliminate on or off chip inductors, which occupies large die or board area respectively.
However, inductors are often necessary for input matching and filtering purpose. Therefore, elimination must take into account system performance degradation. This Chapter also presents the design of low power UWB receiver targeting UWB bandwidth of 3.1GHz to 9.6 GHz in IBM 130 nm 8-RF CMOS technology. Receiver presented consumes 240 mw at 1.2 V power supply, occupies 1 mm$^2$ of die area and meets MB-OFDM UWB systems specifications. Finally, chapter 7 concludes with the status of the current work and future tasks.
CHAPTER 2

WIRELESS COMMUNICATION FUNDAMENTALS

2.1 Introduction

The electromagnetic wave in wireless communication encounters various impediments. These impediments include terrain and objects in the path of the propagating electromagnetic wave, reflections, and distance between receiver and transmitter. These impediments can alter the power of the electromagnetic wave at any point in space. Following sections provide a brief overview of the wireless communication.

2.2 Free Space Propagation and Path Loss

In an idealized wireless link where there are no reflection, scattering and diffraction along the path between the transmitter and receiver, the relationship between the received power $P_R$ and the transmitted power $P_T$ is given by Friis equation:

$$\frac{P_R}{P_T} = G_T G_R L_P$$ (2.1)

where $L_P$ is the path loss, $G_R$ and $G_T$ are the receiver and transmitter antenna gains respectively. The path loss $L_P$ in free space is given as:

$$L_P = \left(\frac{\lambda}{4\pi l}\right)^2 = \left(\frac{c}{4\pi f}\right)^2$$ (2.2)
where $d$ is the distance between transmitter and receiver, $f$ is the signal frequency, $\lambda$ is the signal wavelength and $c$ is the speed of light in vacuum ($=3 \times 10^8 \text{ m/s}$). Above mentioned Friis equation can only predict free space loss for line-of-sight communication such as point-to-point radio link, satellite-to-satellite link, or earth-to-satellite link.

### 2.2.1 Multipath and Fading

Wireless communication between different end-users may encounter various reflective, refractive and scattering objects as shown in Figure 2.1. As a result of these reflections, scattering and diffractions, more than a single communication path between the transmitter and receiver can be present at one time. These multiple signal paths create phase delays in the transmitted signal, which can cause constructive or destructive interference at the receiver. Therefore, total received signal power fluctuates and this fluctuation caused by multipath is known as fading.

*Figure 2.1 Typical indoor and outdoor wireless communication [36]*
2.3 **Receiver Architecture**

Typical radio receivers down convert the modulated radio frequency (RF) signal to baseband by multiplying received signal with a local oscillator (LO) signal. Demodulator, usually a digital circuit, extracts the original information from the baseband signal. To restore the original signal, receiver must provide signal of adequate strength. As a result, receiver must provide enough gain to the received signal without introducing any noise of its own. Furthermore, receiver should spread the gain over the RF, IF and baseband stages to avoid instabilities. Receiver must also need to perform channel selectivity to reject interfering signals. This can be accomplished by using bandpass filter at the RF stage of the receiver and lowpass channel select filter at the baseband of the receiver before demodulation. Following subsections present the two most popular receiver architectures.

2.3.1 **Heterodyne Architecture**

The heterodyne architecture is the most commonly used architecture for communication receiver. Figure 2.2 and Figure 2.3 presents the receiver architecture and frequency transformation in the receiver. The first block in the receiver signal path is a bandpass filter, which suppresses unwanted signals lying outside the RF band of interest. A LNA amplifies the filtered signal with the minimum noise contribution. The mixer multiplies the amplified RF signal with the local oscillator (LO) signal. An IF filter performs channel selection and second mixer transform this signal to baseband. Subsequent blocks perform further filtering, amplification and analog to digital conversion for digital modulator to successfully detect the original transmitted signal.
2.3.2 Direct Conversion Architecture

A direct conversion or zero-IF receiver, illustrated in Figure 2.4, eliminates the IF stages present in heterodyne architecture by setting the local oscillator signal to the same frequency as the desired RF signal. Thus, this architecture directly converts RF signal to baseband as shown in Figure 2.5.
Different standardized metrics measure performances of a receiver. Following subsections presents definitions of the performance metrics used to characterize a receiver.

2.4 Receiver Performance

Different standardized metrics measure performances of a receiver. Following subsections presents definitions of the performance metrics used to characterize a receiver.

2.4.1 Noise Figure and Sensitivity

*Noise figure.* Noise factor measures degradation of the signal to noise ratio as it passes through a component. The noise factor of a two-port network is as follows:
\[ F = \frac{SNR_{in}}{SNR_{out}} \]  

(2.3)

where \( SNR_{in} \) and \( SNR_{out} \) are the signal-to-noise ratios at the input and output respectively. The noise figure (NF) is the noise factor expressed in decibel as given below:

\[ NF = 10 \log_{10} \frac{SNR_{in}}{SNR_{out}} = 10 \log F \]  

(2.4)

In a typical wireless receiver, input signal travels through a cascade of different components such as filter, LNA, and mixer. Each of these components progressively degrades signal to noise ration. Noise factor of a cascaded system with \( n \) components with each component having different noise factor and gain is given by:

\[ F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \cdots + \frac{F_n - 1}{G_1G_2 \cdots G_{n-1}} \]  

(2.5)

where the subscripts refer to stages numbered sequentially from input to output.

**Sensitivity.** The sensitivity of a receiver is defined as the minimum signal level that the receiver can detect. It depends on the thermal noise of the input source resistance, the noise figure, the signal bandwidth and the required signal-to-noise ratio for signal detection. The sensitivity is given by [22]:

\[ P_{\text{min, dBm}} = P_{\text{RS(dBm/Hz)}} + NF_{dB} + 10 \log B + SNR_{\text{min, dB}} \]  

(2.6)

2.4.2 **Linearity**

The linearity of a receiver can be expressed in terms of 1 dB compression point (CP). It is defined as the input signal level that causes small-signal gain to drop by 1 dB. The DR can be expressed as the difference between the 1 dB CP and the minimum
detectable signal (MDS) level. As shown in Figure 2.6, 1 dB CP limits the dynamic range (DR) of the receiver. Note that 1 dB CP is the result of the small signal gain compression.

$$\text{DR} = \text{P}_{1\text{dB}} - \text{MDS}$$

(Figure 2.6 Definition of 1 dB compression point)

In addition, large unwanted signals also compress the gain of the desired weak signal at the receiver, limiting the dynamic range of the receiver.

2.4.3 Inter-modulation Distortion

Almost all system components exhibit non-linear characteristics. In most general case, non-linear circuit response can be expressed in terms of Taylor series expansion:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$$
and considering two input signals with closely spaced frequencies and differing amplitudes,

\[
x(t) = A_1 \cos \omega_1(t) + A_2 \cos \omega_2(t)
\]

(2.9)

the response of the non-linear system can be expressed as:

\[
y(t) = \alpha_1 (A_1 \cos \omega_1(t) + A_2 \cos \omega_2(t)) + \alpha_2 (A_1 \cos \omega_1(t) + A_2 \cos \omega_2(t))^2 \\
+ \alpha_3 (A_1 \cos \omega_1(t) + A_2 \cos \omega_2(t))^3
\]

(2.10)

Expanded expression of the above equation reveals presence of frequency components \((m \omega_1 + n \omega_2)\), which are not present at the input and are known as inter-modulation distortion. Discarding dc terms and harmonics, we obtain the following inter-modulation (IM) products:

\[
\begin{align*}
\omega &= \omega_1 \pm \omega_2 : \alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2)(t) + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)(t) \\
&= 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_1 + \omega_2)(t) + \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_1 - \omega_2)(t) \\
&= 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_1 - \omega_2)(t) + \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_1 + \omega_2)(t)
\end{align*}
\]

(2.11)

(2.12)

(2.13)

and the original signal components:

\[
\begin{align*}
\omega &= \omega_1, \omega_2 : (\alpha_1 A_1 + \frac{3}{4} \alpha_2 A_1^3 + \frac{3}{2} \alpha_3 A_1 A_2^2) \cos \omega_1(t) \\
&= (\alpha_1 A_1 + \frac{3}{4} \alpha_2 A_1^3 + \frac{3}{2} \alpha_3 A_1 A_2^2) \cos \omega_2(t)
\end{align*}
\]

(2.14)

(2.15)

The IM products generated by a non-linear system can appear in the vicinity of \(\omega_1\) and \(\omega_2\), when the difference between \(w_1\) and \(w_2\) is small, distorting the desired signal.
Equation 2.11 shows that third order IM product is proportional to $A^3$. As a result, IM product is small for small input but increases rapidly for large input compared to linear product, which rises slowly for increasing input power. The hypothetical intersection point, where first order power is equal to third order power, is called third intercept point (IP3) as illustrated in Figure 2.8.

Figure 2.7 Output spectrum of second and third order IM products

Figure 2.8 Definition of IIP3
The spurious free dynamic range (SFDR) is defined as the maximum output signal power for which power of the third order inter-modulation product is equal to the noise level of the component. The relationship between IP3 and SFDR is as follows:

\[
SFDR = \frac{3}{2} (IP_3 - MDS)
\]  

(2.16)

where MDS is the minimum detectable signal. The third order intercept point of a cascaded system is given by:

\[
IIP_3 = \frac{1}{\frac{1}{IIP_{3,1}} + \frac{1}{G_1} + \frac{1}{IIP_{3,2}} + \ldots + \frac{1}{G_n} \cdot \frac{1}{IIP_{n}}}
\]  

(2.17)

where subscripts denote IIP3 and gain of the cascaded stages.

2.4.4 I/Q Mismatch

Most of the modern wireless systems use quadrature modulations. Therefore, receiver needs to separate I and Q signals at the input. This is usually accomplished by quadrature mixing by the shifted LO signals as shown in Figure 2.9. The mismatches in I and Q signal paths and the phase shift error from nominal 90° between LO signals corrupt the down-converted signal raising the bit error rate.

![Figure 2.9 Quadrature generation](image)

Figure 2.9 Quadrature generation
With received signal $V_{in}(t) = I(t) \cos \omega_c \ (t) + Q(t) \sin \omega_c \ (t)$, and amplitude and quadrature phase imbalance of $\varepsilon$ and $\mu$, respectively, the baseband $I$ and $Q$ voltages are given by [41]:

$$V_I = I(t) \left(1 + \frac{\varepsilon}{2}\right) \cos\left(\frac{\theta}{2}\right) - Q(t) \left(1 + \frac{\varepsilon}{2}\right) \sin\left(\frac{\theta}{2}\right)$$  \hspace{1cm} (2.18)

$$V_Q = I(t) \left(1 - \frac{\varepsilon}{2}\right) \sin\left(\frac{\theta}{2}\right) + Q(t) \left(1 - \frac{\varepsilon}{2}\right) \cos\left(\frac{\theta}{2}\right)$$  \hspace{1cm} (2.18)

Above equations quantifies down-converted signal corruption due to phase and gain mismatches. Figure 2.10 shows QPSK signal constellation affected by gain and phase errors.

**Figure 2.10** Effect of I/Q mismatch on QPSK signal (a) gain error, (b) phase error [22]
CHAPTER 3

UWB COMMUNICATION BACKGROUND

3.1 Introduction

Wireless communication typically consists of a modulator at the transmitter and demodulator at the receiver as shown in Fig. 3.1. Modulator at the transmitter converts the low frequency baseband signal to higher frequency for transmission of the signal in the air. Wireless transmission considerations include: (1) antenna size (higher the frequency of transmission smaller the antenna); (2) channel characteristics; (3) compliance of FCC for spectrum use.

![Typical Communication Systems](image)

*Figure 3.1 Typical Communication Systems*

Demodulator at the receiver performs the inverse operation of the modulator to extract the original baseband signal with highest accuracy i.e. low distortion, noise, and inter symbol interference (ISI).
This chapter provides detailed background about UWB wireless communication including channel capacity, modulation scheme, multi-path robustness etc. In addition, we discuss multi-band orthogonal frequency division multiplexing in UWB based system design.

3.2 Brief History of UWB Development

Ultra-wideband communications dates back to early 1900. The very first wireless transmission, via the Marconi Spark Gap Emitter, created by the random conductance of a spark was essentially a UWB signal since the instantaneous bandwidth of spark gap transmissions vastly exceeded their information rate. However, the potential of large bandwidth and the capability of multiuser systems provided by electromagnetic pulses remained unexplored until 1960’s, when modern pulse-based transmission gained momentum in military applications in the form of impulse radars [6].

Modern era in UWB began in the early 1960s as a result of the pioneering works in time domain electromagnetic by Harmuth at Catholic University of America, Ross and Robins at Sperry Rand Corporation, and van Etten at the United States Air Force (USAF) Rome Air Development Center [8]. The core idea advanced by these pioneers is to characterize linear, time-invariant (LTI) systems by the output response to the input impulse excitation instead of conventional swept frequency response (i.e. amplitude and phase measurement versus frequency) [7]. The output $y(t)$ of LTI system to an input excitation of $x(t)$ is given by the well known convolution integral:

$$y(t) = \int_{-\infty}^{\infty} h(\tau)x(t-\tau)d\tau$$  \hspace{1cm} (3.1)
\[ h(t) \]

where \( h(t) \) is the impulse response of the system.

The major breakthrough in UWB communications occurred as a result of the invention of sampling oscilloscope by Hewlett Packard in 1962 providing a method to display and integrate UWB signals. In addition, above-mentioned invention also led the way to develop simple circuits necessary for sub-nanosecond, baseband pulse generation.

A decade later, in 1972, the invention of a sensitive baseband pulse receiver by Robbins led to the first patented design of a UWB communications system by Ross at the Sperry Rand Corporation [8]. For the decades following Ross’s invention, UWB technology was restricted to military and Department of Defense (DOD) applications under classified programs such as highly secured communications.

Recent advancement in microprocessors and fast switching in semiconductor technology has made UWB technology viable for commercial applications. As interest in the commercialization of UWB has increased over the past several years, the FCC, in 2002, approved the First Report and Order (R&O) for commercial use of UWB technology under strict power emission limits for various devices.

3.3 Bandwidth Property of UWB Signals

UWB transmits information using very short pulses requiring a very wide instantaneous bandwidth. FCC defines UWB signal as a signal with minimum bandwidth of 500 MHZ or a fractional bandwidth of at least 0.20 as measured from the -10db emission point. Fractional bandwidth \( B_f \) is defined as

\[
B_f = \frac{2(f_h - f_l)}{(f_h + f_l)}
\]  

(3.2)
where

\[ f_u \text{ is the upper frequency measured -10 dB below peak emission point} \]

\[ f_l \text{ is the lower frequency measured -10 dB below peak emission point} \]

The Federal Communication Commission (FCC) allocated 7.5 GHz of unlicensed spectrum bandwidth from 3.1 GHz to 10.6 GHz for UWB communications under strict emission limit. Figure 3.2 shows spectral masks for indoor application.

*Figure 3.2 Spectral Mask for Indoor Applications*

As shown in Figure 3.2, UWB signals may be transmitted at power spectral density (PSD) levels up to -41.3 dBm. This limit on emission allows coexistence of existing 802.11a and WiMax users in the overlapping frequency bands. Figure 3.3 shows spectral masks for outdoor application.
As shown in Figure 3.3, out of band outdoor UWB signals have higher attenuation than indoor UWB signals to reduce interference of GPS signals centered at 1.6 GHZ to ensure that GPS services can coexist with UWB system.

3.4 **UWB Channel Capacity**

As mentioned above, UWB occupies large instantaneous bandwidth. As a result, UWB technology offers substantial increase in channel capacity, which can be perceived from well-known Shannon's link capacity formula:

\[ C = B \log_2(1 + SNR) \]  \hspace{1cm} (3.3)

The link capacity is linearly proportional to the bandwidth and follows a logarithmic relationship with the signal to noise ratio (SNR). Due to linear relationship between channel capacity and bandwidth, a very small radiation power is needed to achieve high data rate when the signal bandwidth is large. Compared to narrowband system, where
high transmission power level is used to maximize data rate, UWB system maximize data rate by transmitting signal over a large frequency range at low power level.

3.5 UWB Signal Shape

As stated above, UWB systems spreads the transmitted power over an extremely large frequency band and thus have a very small transmitting PSD. The frequency domain spectral content of a UWB signal depends on the pulse waveform shape and the pulse width. The most common UWB signals include Gaussian pulse, Gaussian monocycle, Gaussian doublet, Raleigh monocycle and rectangular waveforms. “Gaussian Waveforms” are the most popular choice for UWB communication because of the ease of generation of sub-nanosecond Gaussian pulses. A generic Gaussian pulse shown in Figure 3.4 is defined as

\[ P_g(t) = Ae^{-\left(\frac{t}{\tau}\right)^2} \]  

(3.4)

where

A is the pulse amplitude in volts

\( \tau \) is the pulse width in seconds

\( t \) is the time in seconds
Differentiation of Gaussian pulses once and twice leads to the generation of Rayleigh monocycle and Gaussian monocycles respectively as shown in Figure 3.4. As the order of differentiation increases, number of zero crossing points increases decreasing bandwidth of the signal. PSD of the commonly used pulses is shown in Figure 3.5 below
3.6. UWB Modulation Schemes

Transmission of signal through a communication link requires modulation of the pulses. Four most popular modulation techniques used for UWB communication are On-Off Keying (OOK), Pulse Position Modulation (PPM), Pulse Amplitude Modulation (PAM) and Binary-phase shift keying (BPSK). However, BPSK modulation has a 3db performance advantage over the OOK and PPM modulations.

3.6.1 Pulse Position Modulation (PPM)

PPM is a time-based modulation technique where delay of the pulse carries information about the data. For a binary PPM method, data bit “1” is sent with time shift added to the reference pulse while data bit “0” is sent without any time shift to the reference pulse. Binary PPM is defined as

\[ s(t) = \sum_{n=-\infty}^{\infty} p(t - nT_f - \delta_n) \]  

(3.5)
where \( b_n \in \{0,1\} \) data bits

\( \delta \) is the time shift

\( p(t) \) is the UWB pulse shape

\( T_f \) is the frame time.

![Figure 3.6 PPM Modulation](image)

The advantage of PPM is that it is an orthogonal signaling scheme and uses independent pulses to carry information. Many positions can be used to increase the number of symbols and hence we can have an M-array PPM. However, M-array PPM suffers from inter-symbol interference (ISI) at higher data rates since multiple positions are required for high data rate. Therefore, pulse data rate should be further lowered in case of dense multipath environment to avoid further increase in bit errors due to overlap of the data at the receivers. Performance of PPM in dense multipath is poor even with low data rate. BER performance of PPM is given by

\[
P_e = Q \left( \sqrt{\frac{E_b}{N_0}} \right) \tag{3.6}
\]

where

\( P_e \) is the Probability of error

\( Q \) is the Q-function

\( E_b \) is the average energy per bit (Joules)
\( N_o \) is the noise energy spectral density at the detector (Joules/Hz)

### 3.6.2 On-off Keying (OOK)

In On-Off keying (OOK), the presence of a pulse defines “1” while the absence of a pulse defines “0” as shown in Figure 3.7. OOK is defined as

\[
s(t) = \sum_{n=-\infty}^{\infty} b_n \left( t - nT_f \right)
\]

(3.7)

where

- \( s(t) \) is the UWB signal
- \( b_n \in \{0,1\} \) data bits
- \( p(t) \) is the UWB pulse shape
- \( T_f \) is the frame time.

**Figure 3.7 OOK Modulations**

Advantage of OOK is easy implementation since only one impulse generator is needed but it has poor BER performance just like PPM. BER performance of OOK is same as PPM and is given by

\[
P_e = Q \left( \sqrt{\frac{E_b}{N_o}} \right)
\]

(3.8)
3.6.3 Pulse Amplitude Modulation (PAM)

In PAM, amplitude of a transmitted pulse carries information about the data. Power of the pulses defines the values of the data. For example, 8-array PAM uses eight levels of pulse amplitudes to yield four bits. Two antipodal pulses define binary amplitude modulation similar to BPSK.

![Figure 3.8 PAM Modulations](image)

3.6.4 Binary Phase Shift Keying (BPSK)

In BPSK, a positive pulse defines “1” and a negative pulse defines “0” as shown in Figure 3.9 below. BPSK is defined as

\[ s(t) = \sum_{n=-\infty}^{\infty} b_n(t - nT_s) \]  

(3.9)

where

\[ b_n = \{1,-1\} \] data bits

![Figure 3.9 BPSK Modulations](image)
Disadvantage of BPSK is that two pulse generator is required. However, BPSK has better BER performance compared to PPM and OOK modulation for the same average bit energy level. BER performance of BPSK is given by

$$P_e = Q\left(\frac{2E_b}{N_0}\right)$$

(3.10)

3.7 UWB Signal Detection

Demodulator at the receiver performs the function of extracting the original data information from the modulated pulse trains with highest level of accuracy while reducing transceiver complexity. Typical receiver for UWB signal, which operates in carrier-less fashion, is either autocorrelation or rake receiver.

Correlation receiver first performs the operation of match filtering of the incoming waveform i.e. the incoming signal is matched with a waveform template and the result is integrated. Optimal detection using matched filtering also known as coherent detection requires phase synchronization between the carrier of received signal and oscillator output at the receiver. Figure 3.10 illustrates optimum detection using a correlator.

![Optimum Signal Detection using a correlator](Image)

Detected signal $y(Tb)$ at the output of the correlator can be modeled as:
Where,

\[ x(\tau) \] is the input signal

\[ p(\tau) \] is the known pulsed signal

UWB receiver performs correlation operation between the received signal and the waveform template for each possible pulse position and the correlation results are sent to the baseband for further processing. In absence of multiple access interference, the received signal \( r(t) \) can be modeled as:

\[ r(t) = s(t) + n(t) \] (3.12)

where

\( s(t) \) is the transmitted monocycle

\( n(t) \) is the zero mean white Gaussian noise with power spectral density \( N_0/2 \).

UWB system employs coherent detector as coherent detector provides lower bit error rate than do non-coherent counterpart [22].

### 3.8 UWB Spectral Efficiency

Detection of data at the receiver with certain bit error ratio requires certain level of signal to noise ratio per bit, \( \frac{E_b}{N_o} \). The following equation relates input signal to noise ration (SNR), symbol rate, bandwidth, and corresponding \( \frac{E_b}{N_o} \).
\[
\frac{E_b}{N_o} = \frac{BW}{R_c} \cdot SNR_{in}
\]  

(3.13)

where

- \(BW\) is the signal bandwidth
- \(R_c\) is the symbol rate
- \(\frac{BW}{R_c}\) is the spectral efficiency

We can infer from the above-mentioned relationship that larger input SNR would allow higher spectral efficiency for the same \(\frac{E_b}{N_o}\). In addition, \(\frac{E_b}{N_o}\) also affects demodulator's signal detection efficiency i.e. higher \(\frac{E_b}{N_o}\) ratio lowers bit detection error at the receiver.

Figure 3.11 shows the bit error rate (BER) performance of different modulation schemes mentioned above.

![Figure 3.11 BER for UWB Modulations](image_url)
As seen from the figure above, BPSK outperforms PPM and OOK at the expense of complicated pulse generation circuit. Another commonly used parameter is processing gain (PG), which is defined as the ratio between input SNR and detector $\frac{E_b}{N_0}$. PG can also be defined as the ratio of the channel symbol rate $R_c$, to the bit rate $R_b$:

$$ PG = \frac{R_c}{R_b} $$

(3.14)

Direct sequence spread spectrum (DSSS) coding technique spreads information bit over several pulses or chips to achieve higher processing gain. For example, if the required PG is 20 dB, the system will require a hundred PN chips for each bit of data. Consequently, the data rate is a function of pulse rate and processing gain.

$$ Data\_Rate = \frac{R_c}{Num\_PN\_chips} $$

(3.15)

When the processing gain is unity, the data rate is equal to channel chip rate $R_c$. If $R_c$ is halved and input SNR remains fixed, the PG can also be halved as long as it is still larger than unity so that the data rate remains the same. However, the pulse energy needs to be increased by the same ratio in order to keep the same input SNR.

Figure 3.12 illustrates the relationship between input SNR and system throughput for different modulation schemes for chip rate of 10MHZ in AWGN channel. As shown on the figure, the data rate saturates as the input SNR goes higher than a certain level. The reason is that PG is not needed beyond that point, where the optimal throughput is achieved for that input SNR. However, UWB systems can achieve high data rate and high processing gain simultaneously [4].
Figure 3.12 SNR vs. Throughput for Different Modulation

3.9 UWB Multiple Access Techniques

Modulation and detection techniques described above enable communication between a single receiver and a single transmitter. Network with multiple users requires multiple access techniques. UWB based radio is well suited for multiple access communication due to its large bandwidth. The two common multiple access schemes employed with UWB are Time-Hopping UWB (TH-UWB) [9, 10] and Direct Sequence UWB (DS-UWB) [11].
In TH-UWB, unique time hopping codes are used to position each of the UWB pulses within a given time frame of a particular bit. To support multiple access using TH-UWB, each user is assigned a unique time hopping sequence. In DS-UWB, the PN spreading sequence is multiplied by an impulse sequence. To support multiple access using DS-UWB, each user is assigned a unique PN sequence. In both TH-SS and DS-SS one information bit is spread over various monocycles and requires processing gain for signal detection at receiver.

Once data is modulated using either TH-UWB of DS-UWB techniques, different transmission schemes can be used to broadcast the data. UWB transmission schemes can be broadly categorized as either single carrier or multi-carrier types. Choice of transmission scheme employed in UWB wireless network depends on the following properties: robustness to multi-path fading and robustness to narrowband jammers.

### 3.9.1 Robustness to Multipath Fading

Multiple fades are always present as the UWB occupies a rather large bandwidth from 3.1 - 10.6 GHz. In a single carrier transmission scheme, the digitally modulated baseband signal is transmitted after it is up-converted using one carrier. At the receiving end of the single carrier transmission, multi-finger RAKE receiver is usually employed to counter the effects of multipath fading [12]. The number of fades the receiver can experience over its entire bandwidth determines the number of RAKE fingers used. Therefore, the complexity of the RAKE receiver rise significantly as the UWB system spectrum can have large number of fades present [13].

In a multi-carrier transmission system, the modulated (such as QPSK) baseband signal consists of multiple carriers. These modulated multiple carrier signal is up-
converted prior to transmission. The multi-carrier transmission system can maintain link even in the presence of frequency selective fade, which only remove a few subcarriers. Robustness of single and multi-carrier system against fading is shown in Fig. 3.13.

![Figure 3.13 Impact of fading on single carrier and multi-carrier transmission](image)

**Figure 3.13** Impact of fading on single carrier and multi-carrier transmission

### 3.9.2 Robustness to Narrowband Jammers

In UWB spectrum, various narrowband jammers such as 802.11a, WiMax and marine radar are present. Single carrier system may not be able to maintain link quality in the presence of high power jammers as it will overwhelm the desired signal. However, multi-carrier systems are less susceptible to narrowband jammers as the jammers can only cause selective data loss and error correction techniques can be implemented to mitigate the loss of information.
3.10 Orthogonal Frequency Division Multiplexing

Traditional multi-carrier system divides the spectrum into N non-overlapping sub-channels and extra spacing between the sub-channels is introduced to reduce Inter Symbol Interference (ISI), as shown in Fig. 3.14. As a result, loss of valuable spectrum and drop in spectral efficiency occur.

![Figure 3.14 Traditional Multi-carrier Transmission System](image)

To increase the spectral efficiency of multi-carrier transmission systems, orthogonal frequency division multiplexing OFDM [14] was proposed. In OFDM, a multitude of sinusoids represents a baseband symbol. These sinusoids also bears modulation pattern, such as Quadrature Phase Shift Keying (QPSK). Modulated baseband signal is then up-converted and transmitted in bursts. Mathematically, this up-conversion process is similar to multiplication of baseband symbol by a rectangular pulse. Since each subcarrier is multiplied by a rectangular function in the time domain, the frequency spectrum of each subcarrier looks like a Sinc function, as shown in Fig. 3.15.
As seen from Fig. 3.15, nulls in the spectrum occur at integer multiples of $1/T_s$. Given that all subcarriers have an integral number of cycles within the symbol time $T_s$, only one subcarrier can peak at a time while other sub-carriers will have nulls. This is the property that gives rise to the orthogonality of carriers. Spectrum of OFDM symbol, which comprised of several sub-carriers, is shown in Fig. 3.16.

An OFDM symbol can be represented mathematically as

$$S(t) = \text{rect}\left(\frac{t + \psi}{T_s}\right) \sum_{n=0}^{N-1} \text{Re}\{\exp(j2\pi(f_c + n\Delta f)t)\}$$

(3.16)

where $T_s$ is the symbol time period.
\( f_c \) is the center frequency

\( \Delta f \) is the subcarrier spacing

\( N \) = total number of subcarriers

As mentioned above, OFDM, multi-carrier based system, offers robust performance against multi-path fading and narrow band jammers. Furthermore, OFDM also significantly reduces inter symbol interference due to orthogonality of the subcarriers. OFDM does have some disadvantages: susceptibility to frequency shifts and Peak to average ratio.

**Susceptibility to frequency shifts.** As OFDM relies on orthogonality of subcarriers, a frequency offset, caused by either by phase noise in frequency synthesizer or Doppler shifts, in the subcarriers can cause the link to degrade. To mitigate the impact of phase noise, OFDM receivers generally have very stringent phase noise requirements. Mitigation of deleterious impact of Doppler shifts, which occurs due to relative speed of receiver and transmitter, requires very careful system analysis.

Doppler shift on sub-carriers is as follows:

\[
f_D = \frac{v_r f_c}{C} \cos \alpha
\]  

(3.17)

where

\( f_D \) = frequency deviation due to Doppler Effect

\( v_r \) = relative speed of the transmitter and receiver

\( f_c \) = center frequency of the subcarrier

\( C \) = speed of light

\( \alpha \) = angle of the velocity vector
Doppler effect changes the frequency of all the subcarriers by the same percentage, which destroys the orthogonality of OFDM. Therefore, the relative speeds of the transmitter and the receiver needs to be taken into account in allocating subcarrier spacing. To avoid performance degradation by Doppler shifts, the subcarrier spacing needs to be large and be carefully analyzed.

*High peak to average ratio (PARR).* OFDM system often has PARR in the range of 10-20 dB. It means that average transmitted power is significantly lower to peak transmitted power. As a result, power amplifier (PA) at the transmitter, which is the highest power consuming circuit in transmitter, must be designed to handle those infrequent high peak transmission requiring PA to operate significant back-off from the maximum transmit power. In such PA usage, its efficiency tends to be very low.

### 3.11 UWB Multi-band OFDM

In the Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) version [5] of UWB technology, 128 orthogonal subcarriers, with a subcarrier spacing of 4.125 MHz, comprise 528 MHz wide OFDM signal as shown in Fig. 3.17. In addition, each of these sub-carriers is modulated by Quadrature Phase Shift Keying (QPSK) modulation technique to allow low resolution baseband analog-to-digital (A/D) and digital-to-analog (D/A) converters (4-5 bits).
To enable operation of multi-user operation of UWB systems, the carrier hops around in frequency. The carrier can hop to anyone of fourteen channels \( (2904 + 528n \text{ MHz}, n = 1, 2 \ldots 14) \) as shown in Fig. 3.18. MB-OFDM frequency hopping interval (symbol interval) is 312.5 nS with 9.47 nS guard interval for transmit/receive turnaround time.

Fourteen channels also form sub-groups among them to allow faster implementation of technology using only limited number of sub-groups. Furthermore,
formation of different sub-groups allows flexibility to regulators to control spectrum available for UWB devices, which can be programmed to avoid hopping to parts of the spectrum that are not allocated for UWB. Sub grouping also facilitates easier implementation of some parts of the hardware since the instantaneous bandwidth is only 528 MHz.

For all MB-UWB compliant devices, operation in Band Group 1 is mandatory. A MB-OFDM system operating only in Band Group-1 only is known as Mode-1 systems. To improve system’s robustness against multipath effects and interferences, band hopping is employed within each mode of operation. Representative time frequency interleaving for a Mode 1 system is shown in Fig. 3.19.

![Time frequency interleaving of Mode-1 MB-OFDM system](image)

**Figure 3.19** Time frequency interleaving of Mode-1 MB-OFDM system

Another benefit of MB-OFDM is that the instantaneous SNR of MB-OFDM is high since the carrier hops at a fast rate, which allows instantaneous transmitted signal power to be larger than the average power in a true wideband system.

The major challenge of MB-OFDM hardware implementation is the hardware design since hardware needs to settle within 9.47 nS, which is the guard interval between
hopping. Synthesizer design, in particular, becomes complicated since the Phase Locked Loop (PLL) has to switch frequency within 9.47 nS.

3.12 UWB Multi-band OFDM Specification

MB-OFDM will support high data rate at short distance. The target data rates and distance of operation are summarized in Table 3.1. Timing related parameters are shown in Table 3.2.

Table 3.1 Target data rate and range of MB-OFDM [5]

<table>
<thead>
<tr>
<th>Bit Rate</th>
<th>Distance</th>
</tr>
</thead>
<tbody>
<tr>
<td>110 Mbps</td>
<td>10 m</td>
</tr>
<tr>
<td>200 Mbps</td>
<td>4 m</td>
</tr>
<tr>
<td>480 Mbps</td>
<td>2 m</td>
</tr>
</tbody>
</table>

Table 3.2 Timing parameters of MB-OFDM [5].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nsd: Number of data Subcarriers</td>
<td>100</td>
</tr>
<tr>
<td>Nsp: Number of defined pilot Carriers</td>
<td>10</td>
</tr>
<tr>
<td>Nsg: Number of guard subcarriers</td>
<td>12</td>
</tr>
<tr>
<td>De: Subcarrier spacing</td>
<td>122 ( = NSD + NSP + NSG)</td>
</tr>
<tr>
<td>Tfft: IFFT/FFT Period</td>
<td>242.42 ns (1/De)</td>
</tr>
<tr>
<td>Tzp: Zero pad duration</td>
<td>70.08 ns (=37/528 MHZ)</td>
</tr>
<tr>
<td>Tsym: Symbol internal</td>
<td>312.5 ns</td>
</tr>
</tbody>
</table>

MB-OFDM allows certain frequency hopping sequence within each sub groups to support multiple pico-nets. Four Time Frequency Codes TFCs are available for Groups 1,
2, 3 and 4 devices while only two TFCs are available for Group 5 devices. Table 3.3 shows the TFCs for a Group-1 only system.

Table 3.3 *Time Frequency Codes of Group-1 MB-OFDM System [5]*

<table>
<thead>
<tr>
<th>TFC</th>
<th>Hopping Sequence (Band ID)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 2 3 1 2 3</td>
</tr>
<tr>
<td>2</td>
<td>1 3 2 1 3 2</td>
</tr>
<tr>
<td>3</td>
<td>1 1 2 2 3 3</td>
</tr>
<tr>
<td>4</td>
<td>1 1 3 3 2 2</td>
</tr>
</tbody>
</table>

For Groups 2, 3 and 4 systems, the Band ID should be replaced with numbers appropriate for that group i.e. Band IDs 1, 2 and 3 for a Group-1 system should be replaced with Band ID 4, 5 and 6, for Group 2. PHY parameters of MB-OFDM are shown in Table 3.4.

Table 3.4 *PHY parameters of MB-OFDM [5]*

<table>
<thead>
<tr>
<th>Data Rate (Mbps)</th>
<th>R</th>
<th>Conj Symmetry</th>
<th>TSF</th>
<th>GSPR</th>
<th>CBS</th>
</tr>
</thead>
<tbody>
<tr>
<td>53.3</td>
<td>1/3</td>
<td>Yes</td>
<td>2</td>
<td>4</td>
<td>100</td>
</tr>
<tr>
<td>80</td>
<td>1/2</td>
<td>Yes</td>
<td>2</td>
<td>4</td>
<td>100</td>
</tr>
<tr>
<td>110</td>
<td>11/32</td>
<td>No</td>
<td>2</td>
<td>2</td>
<td>200</td>
</tr>
<tr>
<td>160</td>
<td>1/2</td>
<td>No</td>
<td>2</td>
<td>2</td>
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<tr>
<td>480</td>
<td>3/4</td>
<td>No</td>
<td>1</td>
<td>1</td>
<td>200</td>
</tr>
</tbody>
</table>

where TSF = Time spreading factor, GSPR = Total spreading gain, CBS = Coded bits per OFDM symbol.

### 3.13 Conclusion

This chapter discussed fundamentals of UWB communication. Different pulse shapes and different modulation schemes that could be implemented in UWB systems were discussed. UWB multiple access techniques were also presented. TH-SS UWB and DS-
SS UWB were discussed as two popular methods of multiple accesses in UWB. A
discussion of OFDM and MB OFDM, which offers greater flexibility in UWB system
implementation and which is the focus of this work, were presented.
CHAPTER 4

UWB ARCHITECTURE

4.1 Introduction

Current predominant communication protocols are narrow-band, where a very small fractional bandwidth is used. As an example, popular wireless broadband access protocols, such as 802.11 a/b/g occupies 20 MHZ of frequency spectrum. Mobile telephone protocols, such as Code Division Multiple Axis (CDMA) occupies only 1.2 MHZ of frequency spectrum. As a result, most circuit design techniques and system architectures in existence today complement narrow-band systems and are unsuitable for wideband system like MB-OFDM UWB, where frequency spans 3.1GHZ to 10.6 GHZ. For example, a standard heterodyne architecture requires a band pass filter (BPF) at intermediate frequency, which consumes a large die area in MB-OFDM UWB systems. Standard direct conversion receiver has time varying DC offsets that can degrade performance of MB-OFDM UWB systems.

Similar to architectural level, predominant RF circuit design also complements narrow band systems. For example, RF circuit low noise amplifier (LNA), the most important circuit component in the receiver chain, employs inductive degeneration in narrowband systems. Inductive degeneration makes both amplifier gain and input matching highly frequency selective making it is unsuitable for UWB LNA applications.

Key design constraints that MB-OFDM UWB system design must address are as follows:
1) Wideband Input Matching: RF input matching network must span from 3.1 GHZ to 10.6 GHZ. LNA at the front-end of the receiver need to provide a reasonably low noise figure and high gain while consuming low power. Conventional narrowband LNAs or resistive feedback amplifiers can’t meet these goals [20].

2) Coexistence with other bands: To coexist with other bands in 3.1 GHZ to 10.6 GHZ, second order distortions must be limited. This is due to the fact that second-order distortion in UWB will fall in-band unlike that of narrowband system where such distortions are out of band.

3) Linearity: In wideband receiver, when receiving signal in one channel, signals in other channels enter the receiver and appear as blockers making it vulnerable to cross-band compression. As a result, MB-OFDM UWB receiver needs to meet not only in-band linearity constraints, but also linearity constraints created by cross-band modulation. This problem is illustrated in Fig. 4.1. Suppose the receiver is receiving a weak band 2 (@ 3960 MHZ) signal, a strong out-of-band interferer band 5 (@6864 MHZ) can desensitizes the receiver and degrade the desired signal to noise ratio. In extreme case, all out-of-band channels can be at maximum signal level increasing required linearity level of the receiver. On other hand, in narrowband systems, close-in interferers set the linearity requirements.

*Figure 4.1  Cross Band Compression [21]*
4) LO Spurs and Settling: LO spurs, even the ones that are far away, can down-convert in-band adjacent channels as the wanted band, as shown in Fig. 4.2.

![Figure 4.2 LO Spurs down convert the adjacent channel overlapping the desired signal][21]

Lo settling time in MB-OFMD receiver is also limited to 9.47 ns. Designing synthesizer with frequency range of 3.1 GHZ to 10.6 GHZ with specified settling time is very difficult.

5) Quadrature Accuracy and Filter Linearity: Phase and gain accuracy of quadrature LO is very stringent due to crowded constellation in wideband systems [21]. Channel select filter in MB-OFDM has bandwidth of 264 MHZ and requires ability to handle large signal making it challenging design in low power regime.

Following sections highlights major features of the existing architectures, addresses their viability in MB-OFDM UWB system design, and derives receiver specifications.

4.2 Heterodyne Receiver

Heterodyne receiver down converts the RF signal to intermediate frequency (IF) and then to baseband. Such receiver has unique set of advantages and disadvantages.
Following paragraphs discuss advantages and disadvantages of the heterodyne receivers.

A typical heterodyne receiver is shown in Fig. 4.3.

![Typical Heterodyne Receiver Diagram](image)

**Figure 4.3** Typical Heterodyne Receiver

Advantages of heterodyne receiver are as follows:

1. Reduced DC-Offset: In a heterodyne receiver, LO and RF are at different frequencies and down-conversion occurs in two stages. DC offset in the first down-conversion stage arises mainly due to mismatches in the input circuits and generated offset level is small. A DC blocking capacitor can easily remove the DC offset present at the output of the first down-conversion stage without affecting the desired output signal. However, DC offset does occur in the second down-conversion stage since LO and RF signal frequencies have to be equal to down-convert the received signal to baseband. Nonetheless, this DC offset is very
low since signal gain in excess of 20 db precedes the second down-conversion stage.

2. Improved Distortion Performance: Heterodyne receiver has superior distortion performance since receiver is less susceptible to LO harmonics mixing with harmonics of the received signal. Careful frequency planning can eliminate SNR degradation by pushing harmonic products away from the down-converted signal and filtering the converted signal with a channel select filter at the intermediate frequency level.

3. Inter-stage channel select filter: Heterodyne receiver with fixed Intermediate Frequency (IF) can utilize inter-stage channel select filtering, which can ease adjacent channel suppression requirements of the baseband LPF.

The above-mentioned advantages of a heterodyne receiver make it a very suitable candidate for MB-OFDM UWB receivers. However, it also has some disadvantages. Disadvantages of heterodyne receiver are as follows:

1. Need for an inter-stage filter: In a heterodyne receiver, IF output signal amplitude is high and can easily compress subsequent stages. Therefore, a band pass filter is required at the IF output to ease the linearity requirements on the following IF down-converter chain. This filter needs to suppress the adjacent channels present in a multiple piconet UWB system. On-chip passive band pass filter implementation requires high Q inductors necessitating the use of a thick top metal, which will add to the total cost of the die. On the other hand, active filter implementation requires less die area but it can be very power hungry and can significantly increase noise figure and distortion of the system [15].
2. Need for two LO frequencies: Each of the two down-conversion stages requires a mixer with distinct LO signal. As a result, a heterodyne receiver requires two LO generators, which adds to the total cost of the die.

3. Need for image rejection: In a heterodyne receiver, all received signals have images that can down-convert to the desired channel reducing the SNR of the signal. Fig. 4.4 below illustrates image rejection issue in a heterodyne receiver.

![Image down-conversion in a heterodyne receiver](image.png)

**Figure 4.4** Image down-conversion in a heterodyne receiver

To maintain SNR of the output signal, rejections of images are essential. One or both of the following ways can suppress images in the down converted signals:

1. Front-end image reject filter: An image reject filter at the beginning of the receiver chain can suppress out of band image signal of MB-OFDM systems. For adequate suppression of image signal, images shall be far away from the receive band. With proper frequency planning, a heterodyne receiver can utilize a front-end BPF for suppression of out-of-band image signals.

2. Image reject down-converter: Fig. 4.5 below illustrates an image reject down-converter, which utilizes quadrature phased LO signals to reject the images. Quadrature phased LO signals performs complex signal transformation on the
incoming RF and image signals and image rejection occurs with proper addition of these complex signals. Good image rejection is dependent on maintaining a perfect 90° phase difference between the LO and RF signals and balancing the amplitudes of the RF signal in both branches of the down-converter. The Image Rejection Ratio (IRR) is defined

\[
\text{IRR} = \frac{1}{1 + \delta^2 - 2\delta \cos(\theta)}
\]

where,

*Figure 4.5 Image rejection [16]*

as the ratio of the desired signal amplitude at \(\omega_{LO} - \omega_{RF}\) to the amplitude of the image signal, at \(\omega_{IM} - \omega_{LO}\). The IRR is as follows:

\[
\text{IRR} = \frac{1 + \delta^2 + 2\delta \cos(\theta)}{1 + \delta^2 - 2\delta \cos(\theta)}
\]
\[ \delta = \text{amplitude imbalance of the signal between the two branches} \]

\[ \theta = \text{phase imbalance of the signal between the two branches.} \]

To achieve required 90° phase shift in LO signal, a 90° hybrid coupler or a poly-phase filter can be used. 90° hybrid couplers can be either on-chip or off chip. On-chip implementations of 90° hybrid couplers are difficult to manufacture since they occupy a large die area. As an example, generating a 90° phase shift for a 3 GHz signal would require a very long transmission line (2mm) in Silicon increasing cost of the total systems. Similarly, off-chip chip implementations of 90° hybrid couplers are expensive and increase the cost of the total system significantly.

Active or passive poly-phase filters can also perform 90° phase shift operation on a signal. While active poly-phase filters can have good wideband performance, they usually have poor linearity, high current consumption and high Noise Figure [17] [18]. Passive poly-phase filters use RC poles to perform phase shift operation in the RF signal [19]. However, passive filters in the UWB frequency range (3 - 10 GHz) occupy large die area. For example, creating a RC pole at 3 GHZ would require a capacitor of .53 pF when a resistor of 100 ohm is used. With on-chip capacitors with a density in the range of 2 \( \frac{fF}{\mu m^2} \) in typical CMOS processes, this capacitor would require an area of 265 \( \mu m^2 \).

While area overhead is small for a single RC pole poly-phase filter, a poly-phase filter that operates in the frequency range of 3 GHz to 10 GHz would require multiple RC poles increasing the area overhead. Multi-pole poly-phase RC filter also incurs significant loss in the RF signal [19] severely degrading noise figure of the system. In addition, maintaining amplitude and phase balance, when multiple RC poles are used, are difficult.
due to mismatch in $R$ and $C$ values and circuit parasitic making it unsuitable in MB-OFDM systems.

Generating a signal with frequency of twice the desired LO frequency and then performing frequency division can generate quadrature LO signal. Therefore, Voltage Controlled Oscillator (VCO) in MB-OFDM must operate around 21 GHZ since MB-OFDM signal extends up to 10.5 GHZ. Design of a low power synthesizer that operates at 21 GHz is very challenging.

4.3 Direct Conversion Receiver

Direct conversion receiver down converts the RF signal directly to baseband and is a popular choice for implementation of low-power and low-cost receiver. Typical direct conversion design issues plague the UWB receiver design, except that baseband flicker noise has minor effect. Fig. 4.6. illustrates a direct conversion receiver, along with some issues typically seen in a direct conversion receiver.

\[ \text{Figure 4.6 A Typical Direct Conversion Receiver} \]
Following paragraphs discusses advantages and disadvantages of the direct conversion receivers. Advantages of direct conversion receiver are as follows:

1. **No Image Rejection Filter:** Zero IF direct conversion architecture doesn’t require any image rejection filter since no image signal is created when RF signal is down-converted to zero-IF.

2. **LO scheme simplicity:** Direct conversion zero-IF receiver employs single local oscillator requiring only one frequency synthesizer. As a result, power consumption reduces significantly. Furthermore, both transmit and receiver blocks can share the same synthesizer in direct-conversion receiver. On the other hand, heterodyne receiver can share synthesizer only if transmitter is also a heterodyne transmitter.

3. **Reduced power consumption and die area:** Both power consumption and area overhead is lower for zero-IF direct conversion receiver compared to heterodyne receiver since direct conversion receiver uses fewer components than heterodyne receiver. As an example, a direct conversion receiver requires only one down-converter, while a heterodyne receiver requires two down converters.

Disadvantages of direct conversion receiver are as follows:

1. **DC Offset:** In a direct conversion receiver, both LO and RF incoming signal occupy the same frequency. LO leaking to RF signal can mix with itself to produce DC offset. As an example, in a Gilbert Cell based mixer, the LO can couple to the RF input port through the $C_{gs}$ (gate-source capacitance) and $C_{gd}$ (gate-drain capacitance) and create undesired DC offset. Furthermore, any mismatch in the input differential pairs will create a DC offset at the output of the
circuit. However, employing large device sizes can keep offsets due to mismatch to a minimum. DC offset is one of the biggest issues that plague direct conversion receivers. DC offset in direct-conversion receiver can

a) corrupt output spectrum: In MB-OFDM direct conversion receiver, DC offset is the result of self-mixing of LO with center carrier. As a result, SNR of the signal located at the center carrier degrades compared to signal located farther away from the center carrier distorting the spectrum content of the output signal.

b) compress the baseband Analog-to-Digital converter (ADC): Wideband direct conversion mixer generally employ resistive load to extend bandwidth. Typical value of resistor used in the direct conversion mixer is 100 ohms with peak voltage drop of 1V and current consumption in the range of 10 mA. Therefore, only 0.1% mismatch in the load resistors or in the bias current can produce a 1mV DC offset at the mixer output. As shown in typical MB-OFDM direct-conversion receiver lineup in Fig. 4.7, 1mV DC offset at the mixer output can cause .5V DC offset at the input of the baseband ADC. This DC offset adds to RF signal, which may also be in the range of 1V. This combined signal can easily compress most ADC, which generally operates in the 0.5V to 1V range.
Figure 4.7 Approximation of DC offset in a direct-conversion receiver

To minimize the negative impacts of DC offset, as shown in Figure 4.8, almost all direct conversion receivers employ some kind of a DC offset cancellation schemes, which includes DC offset calibration and DC blocking capacitor:

Figure 4.8 DC offset and second-order distortion issues in direct conversion MB-OFDM receivers
a) DC offset calibration loop: It measures the baseband output signal and feeds back the signal to the mixer input or output to cancel DC offset. Cancellation of DC offset is a slow process making it difficult to be employed in UWB receiver. Furthermore, DC offset changes over time due to change in temperature and change in RF and LO frequencies. This change in DC offset is not an issue for narrowband systems, where the frequency tuning range is relatively small and system operating frequency is static. In contrast, MB-OFDM systems use time-frequency interleaving and operating frequency could change from 3.4 GHz to 10 GHz in less than 400 nS as shown in Fig. 2.16. As a result, DC offset changes significantly every 400nS. In addition, offset calibration has to settle within MB-OFDM guard time interval of 9.47 nS. Designing a DC offset calibration loop that settles within this short time is a tremendous challenge.

b) DC blocking capacitor: Placing DC blocking capacitor at the output of direct conversion mixer is not viable for MB-OFDM receiver because of the degraded output of the desired signal. In MB-OFDM, received signal amplitude changes every 400ns due to differing free space path loss at different hopped frequencies. As an example, a 1MHz pole created by the DC blocking capacitor at the baseband output produces a time constant of 1μS as shown in Fig. 3.3. As a result, receiver will take approximately 1μS to settle at every frequency hop whereas maximum allowed settling time is 9.47 ns in MB-OFDM.
2. Second-order distortion: Second-order distortion is a major concern for MB-OFDM receivers. In MB-OFDM, second-order distortion of in-band channels can also land in-band. In addition, harmonics of the received signal can mix with the harmonics of the LO and down-convert to baseband, creating additional 2\textsuperscript{nd} harmonic distortions. As a result, IIP\textsubscript{2} performance of direct conversion receiver suffers. Higher DC offset of direct-conversion receiver also negatively impacts IIP\textsubscript{2} performance. Consequently, direct-conversion receivers are not as robust as heterodyne receivers in MB-OFDM systems.

3. Baseband Channel Select Filtering: In a direct-conversion receiver, all the channel select filtering occurs after the down-conversion process. Therefore, suppression of adjacent channels requires very sharp cut-off low pass filter i.e. high order filter. In addition, such high order filter must handle large amplitude baseband signal (of the order of 1V). An active implementation of this type of LPF will consume large amount of power [15]. In contrast, baseband LPF in a heterodyne receiver does not have stringent specifications since inter-stage channel select filter (after the first down-conversion stage) relaxes the specifications of the baseband LPF.

4. LO Re-Radiation: In a direct conversion system, both RF signal and LO signal are always in-band and LO signal can leak to transmit path corrupting the spectrum of transmitted signal. In contrast, in a heterodyne receiver, the LO signal and RF signal are at different frequencies. With careful frequency planning, we can select LO in heterodyne receiver to be out-of-band.
This research focuses on a direct conversion. The main objective of this research is to implement a direct conversion receiver that minimizes classical problems of a direct down-conversion receiver. Furthermore, both power consumption and the die area of the design shall be the same or less than that of a heterodyne receiver.

4.4 MB-OFDM UWB Receiver Specifications

Low-cost highly integrated receiver architecture mandates use of minimal number of external components. Direct conversion receiver is most suitable for low cost CMOS implementation. In the proposed direct conversion architecture shown in Fig. 4.9, a single RF chain receives the signal and an off-chip frequency synthesizer generates the required LO. This architecture doesn’t require multiple LNAs to cover the wide bandwidth or require several LO generators, simplifying the overall receiver and eliminating potential problems such as harmonic pulling that arise between multiple VCOs on a chip.

*Figure 4.9* Proposed Receiver Architecture
However, proposed direct conversion architecture suffers from imperfections and mismatches in the RF chain, resulting in undesired signals at DC as well as a fixed-pattern noise at the hopping frequency. Fixed-pattern noise (i.e. varying DC offset) at the hopping frequency occurs due to LO self-mixing as the receiver hops across channels. The design presented here only addresses the offset that lies at DC. The cancellation of the varying DC offset at the hopping frequency is assumed to be handled by digital calibration at the baseband.

The RF receiver signal path includes an external passive pre-filter to reduce the level of out-of-band interferers. Filtered antenna signal pass thru a wideband LNA and a quadrature mixer that converts the signal down to zero-IF. An off-chip synthesizer provides the quadrature LO signals with frequency hopping per MB-OFDM specifications. AC-coupling capacitor connects the output of the mixer and channel select with overall corner frequency of 2 MHZ, removing DC offset. Note that A/C coupling is feasible since 0th subcarrier in MB-OFDM has no signal information. Furthermore, the use of AC coupling capacitor suppresses 1/f noise and DC offset. Output of the ac coupled mixer signal gets filtered at the baseband channel select filter. Output of the filter also interfaces PGA via AC coupling. PGA adjusts the gain in accordance with received signal strength for optimal interface to the baseband ADC. At the end of the receiver chain, the digital baseband processor performs the final signal processing.

Robust UWB communication system requires that the receiver function properly in presence of hostile out-of-band ISM interferes and in-band 5-GHZ UNII interferers. RF SAW pre-filter, which removes out-of-band interferer, and a notch filter centered at 5 GHZ UNII band relaxes receiver dynamic range. Large bandwidth of the UWB signal
forces use of RF front-end with low gain compared to narrow band systems. As a result, baseband channel select filter must have very small input-referred noise. Furthermore, baseband filter requires high attenuation and a very accurate and steep roll-off to further limit interfering signal strength, which limits dynamic range of the subsequent ADC. Synthesizer implementation must limit spurious tones at the output of the synthesizer, which can transform interferers into the wanted frequency band. The remainder of this section deals with more detailed system specifications.

1. Sensitivity, Gain, NF: In MB-OFDM UWB, an UWB receiver operating in the first three bands (Mode 1 only) needs to have a noise figure (NF) better than 6.6 dB. However, for the UWB device operating in the first three band groups with nine bands, the required system NF can be 9 dB taking into account the coding gain. A margin of 3 dB is added to set the NF specification for the receiver as 6 dB. This margin is set after system level simulation taking into account the following combined non-idealities: 1) 5 degrees in phase and 1 dB in amplitude of I/Q imbalance; 2) 5 bits of effective ADC quantization; 3) 9 dB of clipping in the signal peak-to-average ratio (PAR); 4) a signal-to-interference ratio (SIR) of 15dB at baseband (due to in-band interference down-converted by spurs from the synthesizer).

The relationship between sensitivity and NF and SNR is as follows:

\[
\text{Sensitivity} = -174 \text{ dBm} + 10\log (\text{Data Rate}) + \text{NF} + \text{SNR} \quad (4.2)
\]

Minimum SNR required for QPSK modulated MB-OFDM signal for bit error rate of 1E-5 is 8 dB. Therefore, for the specified NF of 6 dB and SNR of 8 dB, sensitivity of the MB-OFDM standard is -73.2 dBm (= -174 dBm + 10*log
\[(480e6) + 6dB + 8dB = -73.2 \text{ dBm}\) for 480 Mb/s over AWGN channel. The RX must provide a maximum voltage gain of approximately 72 dB so as to raise the minimum signal level to the full scale (500 mV P-P i.e. -2 dBm at 50 ohms) of the baseband ADC.

FCC part 15 limit of transmit power for UWB spectrum is \(-41.25 \text{ dBm/MHZ}\). Therefore, maximum transmit signal power for three UWB band is \(-9.25 \text{ dBm} = -41.25 \text{ dBm/MHZ} + 10 \cdot \log(3.528)\). Assuming communication distance of 0.2m, path loss is 34 dB. Therefore, maximum received signal at the antenna is \(-43 \text{ dBm}\). To cover the full dynamic range of the input, automatic gain control is set to 30 dB.

2. Linearity Requirements: The receiver linearity is set by the requirement that UWB receiver have little degradation of signal-to-interference ratio (SIR) in the presence of in-band or out-of-band interferers. For integration of UWB receiver into existing electronic devices such as PCs, printers, HDTVs, cameras, and PDA etc., receiver must be able to suppress strong interferers from the 802.11 WLAN, bluetooth wireless technologies in both 5 GHZ UNII and 2.4 GHZ ISM bands. With proposed maximum distance for a UWB link has been set to 10 meters, minimum received power of the wanted signal is approximately \(-74 \text{ dBm}\). In-band noise power level is \(-80 \text{ dBm}\) as the system noise figure (NF) is 6 dB. The interference criteria assume that receiver operates 6 dB above the sensitivity level. To allow 6-dB margin, the sum of the interferer-and-noise power can be at most be \(-74 \text{ dBm}\).

The largest out-of-band interferer powers from an ISM band (IEEE 802.11 b/g) interferer at 0.2-m could be up to \(-5.8 \text{ dBm}\). Power at received at LNA input is
approximately -40.8 dBm assuming front-end pre-select filter provides 35-dB attenuation at 2.45 GHz. To meet the interferer power requirement (-74 dBm), RX must provide an additional 33.2 dB attenuation of the interference at 2.45 GHz. The above-mentioned 802.11 b/g interferer and other out-of-band interferers (such as PCS, GSM, etc.,) contribute to the receiver P-1dB compression point. Additional filtering in the receiver signal chain can increase receiver P-1dB compression point. To calculate P-1dB, assume transmitter is located within 0.1 m and is transmitting at maximum power level of -9.3 dBm. Maximum received signal power at a MB-OFDM front-end receiver could be -29.5 dBm for three bands. Therefore, P-1 dB compression point must exceed -19.5 dBm to allow for 10-db margin.

In-band IIP3 of the receiver can be derived from the two-tone test equation. As stated before, the desired signal power at the receiver input is -29.5 dBm for communication distance of 0.1m. With two in-band tones at -29.5 dBm, in-band IIP3 = Pin(dB) + ∆P(db)/2.

\[
\text{IIP3 (dBm)} = -29.5 \text{ dBm} + (74-29.5)/2 \text{ dBm} = -7.25 \text{ dBm.} \quad (4.3)
\]

Similarly, in-band IIP2 can also require two-tone test. The worst case IIP2 occurs for a two-tone case, where a second-order difference product falls in-band in the RF front end. For example, assuming an IEEE802.11a band interferer at 0.2-m distance and a PCS/GSM1900 band interferer at 1-m distance have transmit power of 30 dBm, the received interferer power levels are -4 dBm and -8 dBm, respectively. This leads to an IIP2 requirement above -20 dBm when a realistic 20-dB attenuation in pre-filter is taken into account.
3. Synthesizer Requirements: In MB-OFDM UWB system, synthesizer must settle within .5 ns guard interval between frequency hopping. In addition, system requires high purity in the generated carriers due to the presence of strong interferers. To coexist with the 5 GHZ UNII band and 2.4 GHZ ISM band users, spurious tones in the 5 GHz range and 2 GHZ range must be below -50 dBc and -45 dBc respectively. Finally, from system level simulation, VCO phase noise specification is set to -100 dBc at 1 MHz and overall integrated phase noise set at 3.5 degrees rms to allow system SNR degradation of no more than 0.1 dB.

4. Filter and ADC Requirements: As shown in Fig. 2.19, MB-OFDM standard specifies total symbol duration as 312.5 ns including a cyclic prefix extension of 60.6 ns. The cyclic prefix extension alleviates loss of orthogonality of sub-carriers due to multi-path fading and resulting BER. However, analog part of the receiver consumes a portion of the cyclic prefix reducing the overall system robustness against multipath. MB-OFDM UWB receivers usually employ high order (5th order) and relatively sharp cut-off baseband filters for adjacent channel (centered 528 MHz away from the band of interest) in analog domain. This is necessary if the ADC samples the data at the nyquist rate of 528 MHz (signal bandwidth is 264 MHZ in IQ mixer). The main drawbacks of using high order analog filters is that it introduces large in-band group delay and requires large area in passive implementation or requires large power and increased noise for active implementation.

In contrast, if the ADC samples at the rate of 1.056-GS/s (2X oversampling ratio), it will allow implementation of linear phase filtering in the digital domain and lower attenuation requirements of analog filter. With relaxed attenuation, analog filter will
have small group delay variations. As a result, the overall robustness of the system against multipath and in-band interference is enhanced at the expense of increased power dissipation in the ADC. In this design, the above-mentioned LPF and oversampled ADC combination is chosen.

OFDM modulation is robust against amplitude variations among the sub-carriers allowing rejection of the adjacent channel in the digital domain. Therefore, chosen analog LPF attenuates signal at alternate channels while digital filter suppresses signal at adjacent channel. Analog LPF provides sufficient attenuation (centered 1056 MHz away from the band of interest) to limit aliasing by the ADC samples at 1056 MHZ. A fourth-order chebyshev filter is adequate to achieve both attenuation and group delay goals. The chosen fourth order filter can achieve a group delay variation of less than 0.3 ns (5% of the cyclic prefix) and attenuate the alternate band by more than 40 dB. Table 4.1 below summarizes overall specification of the MB-OFDM receiver.

Table 4.1 MB-OFDM Receiver Specification

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>Receiver Gain</th>
<th>72 dB</th>
</tr>
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<tbody>
<tr>
<td><strong>Sensitivity</strong></td>
<td>-73.2 dBm</td>
<td>Overall P1dB</td>
<td>-19 dBm</td>
</tr>
<tr>
<td><strong>Data Rate</strong></td>
<td>480 MBPS</td>
<td>Overall IIP3</td>
<td>-7 dBm</td>
</tr>
<tr>
<td><strong>Channel BW</strong></td>
<td>528 MHZ</td>
<td>Overall IIP2</td>
<td>-20 dBm</td>
</tr>
<tr>
<td><strong>SNR (BER = 1E-5)</strong></td>
<td>8 dB</td>
<td>Total AGC Range</td>
<td>30 dB</td>
</tr>
<tr>
<td><strong>RX NF</strong></td>
<td>6 dB</td>
<td>ADC resolution</td>
<td>6 bits @1GS/s</td>
</tr>
</tbody>
</table>
Gain distribution in RF signal receiver chain trades off IIP3 and NF. Large front-end gain reduces impact of converter noise figure on the total noise figure. However, implementation of large gain LNA in UWB is expensive in terms of power consumption. Furthermore, high gain LNA would require large IIP3 for the subsequent converter and amplifiers leading to large power consumption.

The input match and power consumption consideration restrict LNA gain to 15 dB. To relax the NF requirements of subsequent baseband LPF, the down conversion mixer gain is set to 20 dB for an overall RF front-end gain of 35 dB. With insertion loss of the LPF of -3 db across the pass band, the minimum require gain at PGA is 37 dB. LNA accommodates gain control of 12 dB to avoid excessive non-linearity at subsequent stages. PGA gain ranges from 21 dB to 37 dB to achieve total AGC of 30dB. Table 4.2 below summarizes specification of the MB-OFDM receiver components.

### Table 4.2  **MB-OFDM Receiver Component Specification**

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Gain Range</th>
<th>NF</th>
<th>IIP3</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>15 dB (20dB – 8dB)</td>
<td>4.5 db</td>
<td>-10 dBm</td>
<td></td>
</tr>
<tr>
<td>Mixer</td>
<td>10 dB</td>
<td>15 db</td>
<td>0 dBm</td>
<td></td>
</tr>
<tr>
<td>LPF</td>
<td>-1 dB (fc = 264 MHZ)</td>
<td>20 db</td>
<td>100 dBm</td>
<td>3rd order elliptical</td>
</tr>
<tr>
<td>PGA</td>
<td>37 dB (21dB – 37dB)</td>
<td>20 db</td>
<td>10 dBm</td>
<td></td>
</tr>
</tbody>
</table>

Figure 4.10 shows the input power, noise power and OIP3 levels at each stage of the receiver.
Figure 4.10  Level plan for MB-OFDM UWB receiver
CHAPTER 5

CMOS TECHNOLOGY

5.1 Introduction

CMOS technologies offer the possibility of integrating both baseband and RF front-end components of the receiver on a single chip, allowing low cost implementation. This work utilizes CMOS process. Following subsections provides overviews of basic device modeling parameters including descriptions of passive devices available in IBM 8RF CMOS process used in this work.

5.2 MOS Transistors Modeling

MOS transistor is the basic building block of a circuit. A typical cross section of an NMOS transistor is shown in Figure 5.1.

*Figure 5.1 Cross section of N-channel MOS transistor*
Accurate transistor modeling plays an important role in translation of simulated circuit to successful IC implementation. The transistor modeling in modern CMOS technologies requires consideration of many novel effects. One of the commonly used MOS transistor models is Berkeley Short-Channel IGFET Model, referred as BSIM. This model emphasizes less on the exact physical parameter of the device, but instead focuses on empirical parameters and polynomial equations that address novel effects. The latest version of BSIM model is BSIM4 [37]. BSIM4 models various effects of short channel devices to accurately parameterize measured results.

*Poly-silicon Gate Depletion*

As the technology scales smaller, gate oxide thickness is decreasing. Impact of poly depletion can no longer be ignored. Figure 5.2 illustrates charge distribution in MOSFET with n+ poly gate depletion. The presence of depletion region of poly gate reduces effective gate to source voltage.

![Poly Gate Depletion](image)

*Figure 5.2 Charge distribution in a MOSFET with poly gate depletion* [40]
Taking poly depletion into account, effective gate to source voltage is modeled as:

\[ V_{gs,\text{eff}} = VFB + \Phi_z + \frac{q\varepsilon_{\text{si}} N_{\text{GATE}} \cdot TOX^2}{EPSROX^2} \left( \sqrt{1 + \frac{2EPSROX^2 (Vgs - VFB - \Phi_z)}{q\varepsilon_{\text{si}} N_{\text{GATE}} \cdot TOX^2}} - 1 \right) \]  

(5.1)

**Threshold Voltage Model**

Accurate modeling of threshold is an important parameter for precise characterization of MOSFET. BSIM4 models impacts of non-uniform substrate doping, drain induced barrier lowering and narrow width on device threshold. As an example, threshold voltage of retrograde doped substrate is modeled as:

\[ V_{th} = VTH0 + K1 \left( \sqrt{\Phi_z - V_{bs}} - \sqrt{\Phi_z} \right) - K2 \cdot V_{bs} \]  

(5.2)

In short channel devices, dependence of \( V_{th} \) on body bias becomes weak and shows a greater dependence on drain voltage, which is known as drain induced barrier lowering (DIBL). As a result of DIBL, threshold voltage decreases with increasing drain voltage. In addition, device with narrow width shows increase in threshold due to the presence of fringing electrical field. This effect becomes substantial for as the channel width decreases. BSIM4 models both DIBL and narrow-width effects on threshold.

**Gate Direct Tunneling Current Model**

As the gate oxide thickness decreases, tunneling of carriers either electron or holes occurs between the gate and silicon beneath the gate oxide. BSIM4 models three component of tunneling current as shown in Figure 5.3.
Drain Current, Body Current and Output Conductance Model

Drain current and output conductance of sub-micron MOSFET have four distinct regions of operations: triode region, channel-length modulated (CLM) region, drain induced barrier lowering (DIBL) region, and substrate current induced body effect (SCBE) region. Figure 5.4 illustrates MOSFET operations in these regions.
The complete single equation channel current model, which includes contributions of velocity saturation, CLM, DIBL, SCBE, and drain induced threshold shift (DITS) caused by pocket implantation, is given by [40]:

\[
I_{DS} = \frac{I_{DS0}}{1 + \frac{R_{DS} I_{DS0}}{V_{DSeff}}} \left[ 1 + \frac{1}{C_{CLM}} \ln \left( \frac{V_A}{V_{ASAT}} \right) \right] \left( 1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}} \right) \\
X \left( 1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}} \right) \left( 1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}} \right)
\]

(5.3)

where

\[
V_A = V_{SAT} + V_{ACL}
\]

(5.4)

The current \(I_{DS0}\) in (5.1) is the channel current for an intrinsic device (without source/drain resistance) operating between strong inversion to sub-threshold. \(I_{DS0}\) is given as:

\[
I_{DS0} = \frac{W_{eff} \mu_{eff} C_{ox} V_{gsteff} V_{dseff}}{L_{eff} \left( 1 + \frac{\mu_{eff} V_{dseff}}{2V_{SATeff}} \right)} \left( 1 - \frac{V_{dseff}}{2V_b} \right)
\]

(5.5)

where

\[
V_b = \frac{V_{gsteff} + 2KT/q}{A_{bulk}}
\]

(5.6)

Body current in MOSFET comprises gate-to-body tunneling current, substrate current due to impact ionization, gate induced drain leakage current (GIDL) and source
induced gate leakage current (DISL). Equations for these currents can be found BSIM4 user’s manual [40].

**Non-Quasi-Static Model (NQS)**

Accurate transient and AC analysis must take into account finite channel/gate charge response to external applied voltage. Quasi-static model uses lumped gate capacitor and channel resistance model as shown in Figure 5.5 (b). This ignores finite channel charging time. A way to capture NQS effect is to uses distributed model as shown in Figure 5.5 (c). BSIM4 uses Elmore equivalent circuit model to model channel charge as shown in Figure 5.5 (d).

![Figure 5.5 BSIM4 NQS MOSFET model [40]](image-url)
Gate Resistance Modeling

BSIM4 provides several gate resistance models with selector $RGATEMOD$ to choose among them. When selector $RGATEMOD=1$, gate physical resistance is added to the intrinsic model of the transistor. The value of the resistance is given as:

$$ R_{Glead} = \frac{R_{SHG}(XGW + \frac{W_{eff,CJ}}{3NGCON})}{NGCON(L - XGL)NF} \quad (5.7) $$

where $R_{SHG}$ denotes the sheet resistance of the gate polysilicon, $NGCON$ the number of gate contacts of each finger (the gate finger can have contacts either at one or both sides as shown in Figure 5.6), $XGW$ the distance between the gate contact and the channel edge, and $XGL$ the difference between the $L$.

![Figure 5.6](image)

**Figure 5.6** Gate geometry (a) $NGCON = 1$, (b) $NGCON = 2$
If the gate is contacted at one side \( \text{NGCON}=1 \) (Figure 5.6a), \( XGW=XGL=0 \) and \( NF=1 \), then the equation (5.7) simplifies to:

\[
R_{G_{eltd}} = \frac{1}{3} \frac{R_{SHG}}{L} \frac{W_{eff,CJ}}{L} \quad (5.8)
\]

The factor \( 1/3 \) accounts for the distributed nature of the current conduction [39]. If the gate is contacted from both sides (\( \text{NGCON}=2 \)) is illustrated in Figure 5.6b. If \( XGW=XGL=0 \) and \( NF=1 \), then the equation (5.7) simplifies to:

\[
R_{G_{eltd}} = \frac{1}{12} \frac{R_{SHG}}{L} \frac{W_{eff,CJ}}{L} \quad (5.9)
\]

When selector \( \text{RGATEMOD}=2 \), BSIM4 model uses a "channel-reflected gate resistance" (\( R_{G,crg} \)) in addition to gate resistance \( R_{G,eltd} \). \( R_{G,crg} \) represents the first order non-quasi-static effects in the channel. This gate resistance is given in Equation 5.10. Since this gate resistance is not a physical resistance, it does not include a thermal noise source in the circuit model.

\[
R_{G,crg} = \frac{1}{X_{RCRG1} \left( \frac{I_{ds}}{V_{dseff}} + X_{RCRG2} \frac{kT}{q} \frac{W_{eff}}{L_{eff}} C_{ox,IV} NF \right)} \quad (5.10)
\]
When selector $RGATEMOD=3$, the location of the overlap capacitances changes. The equivalent circuit models for different $RGATEMOD$ settings are shown in Figure 5.7.
**Noise Modeling**

BSIM4 models following types of noise:

1. Flicker noise
2. Channel thermal noise
3. Induced gate noise and correlation with channel thermal noise
4. Shot noise due to the gate tunneling current
5. Thermal noise due to the resistances at the terminals

**Flicker Noise Model**

BSIM4 provides two different flicker noise models with selector $f\text{n}o\text{i}M\text{o}d$ to choose between them. If $f\text{n}o\text{i}M\text{o}d=0$, a simple flicker noise model is used. The drain flicker noise current is given as:

$$
\overline{i_{d}^{2}}_{\text{Flicker}} = \frac{K F (I_{ds})^{AF}}{C'_{ox} L_{eff}^{2} f_{EF}^{2} \Delta f} \Delta f
$$

If $f\text{n}o\text{i}M\text{o}d=1$, a unified flicker noise model is used. The drain flicker noise current is given as [37]:

$$
\overline{i_{d}^{2}}_{\text{Flicker}} \approx f'(NOIA, NOIB, NOIC) \left[ \frac{I_{ds}}{C'_{ox} L_{eff}^{2} f_{EF}^{2}} + \frac{g'(EM) I_{ds}}{W_{eff} L_{eff}^{2} f_{EF}^{2}} \right] \Delta f
$$

**Channel Thermal Noise Model**

BSIM4 provides two options for the channel thermal noise with selector $T\text{N}O\text{I}M\text{O}D$ to choose between them. The charge-based model ($T\text{N}O\text{I}M\text{O}D=0$) defines the channel thermal noise as

$$
\overline{i_{d}^{2}} = \frac{4kT \cdot NTNOI}{R_{DS} + L_{eff}^{2} \left( \mu_{eff} | Q_{inv} | \right)} \Delta f
$$
If $TNOIMOD=1$, the holistic thermal model is used. In this model, all the short-channel effects including the velocity saturation effect incorporated in the I-V model are automatically included in the noise calculation. Additionally the modeling captures the amplification of the channel thermal noise through $gm$ and $gmb$ as well as the induced gate noise with the correlation to the channel thermal noise. The channel thermal noise in the holistic model is given by

\[
\frac{i_d^2}{\Delta f} = 4kT \frac{V_{d_{eff}}}{I_{ds}} (\beta g_m + \beta g_{mb} + g_d)^2 - 4kTR_c (g_m + g_{mb} + g_d)^2
\] (5.14)

Where

\[
R_c = \theta^2 \frac{V_{d_{eff}}}{I_{ds}}
\] (5.15)

\[
\beta = .577X \left[ 1 + TNOIA L_{eff} \left( \frac{\mu g_{seff}}{2VSAT.L_{eff}} \right) \right]^2
\] (5.16)

\[
\theta = .37X \left[ 1 + TNOIB L_{eff} \left( \frac{\mu g_{seff}}{2VSAT.L_{eff}} \right) \right]^2
\] (5.17)

*Shot Noise Model due to Gate Tunneling Current*

The BSIM4 models the shot noise contributed from the gate tunneling current. This shot noise current is given by [38]:

\[
\frac{i_{gtx}^2}{\Delta f} = 2qI_{gtx}
\] (5.18)

where $I_{gtx}$ can be one of the following tunneling currents: the gate-to-source tunneling current, the gate-to-drain tunneling current, or gate-to-substrate tunneling current.
Thermal Noise Models for Parasitic Resistance

BSIM4 models the thermal noise contribution from parasitic resistances at the gate, the drain, the source and the substrate. The thermal noise of the above mentioned sources are given by:

1. Gate resistance
   \[ \frac{i_{RG}^2}{\Delta f} = \frac{4kT}{R_G} \]  
   (5.19)

2. Drain resistance
   \[ \frac{i_{RD}^2}{\Delta f} = \frac{4kT}{R_D} \]  
   (5.20)

3. Source resistance
   \[ \frac{i_{RS}^2}{\Delta f} = \frac{4kT}{R_S} \]  
   (5.21)

4. Substrate resistance
   \[ \frac{i_{R_{Subx}}^2}{\Delta f} = \frac{4kT}{R_{Subx}} \]  
   (5.22)

where \( R_{Subx} \) can be \( RBPS, RBPD, RBSB, RBDB \) or \( RBPB \).

Stress Effect

As CMOS features scales down at or below 130 nm, shallow trench isolation is becoming popular for device isolation to avoid limits of traditional field oxide isolation plagued by bird’s beak. Stress induced by the shallow trenches influences mobility, threshold and saturation velocity since doping profile may change near the trench edges. Devices in close proximity to shallow trenches have the significant profile changes compared to the devices farther from the trenches. BSIM4 models both threshold voltage and mobility changes due to shallow trenches.
5.3 Passive Devices in CMOS

Most commonly used passive device in RF circuits implemented in CMOS process includes capacitors, varactors, and inductors. Followings subsections presents these passive devices.

5.3.1 Capacitors

Capacitors find usage in matching networks, as AC coupling components and as decoupling (blocking) components on the DC lines. Capacitors in RF applications require self resonance frequencies larger than the frequency of operation, high quality factors $Q$, good linearity and large break-down voltage. In integrated RF circuit, both capacitance density and the ratio between the desired capacitance and parasitic capacitance $C/C_{parasitic}$ are the key parameters. Available capacitor types in CMOS include MOS capacitor, Metal-Oxide-Metal (MOM) capacitor, Metal-Insulator-Metal (MIM) capacitor and MOS varactors.

MOS Capacitors

MOS capacitors use the device capacitance between the gate and common source/drain contacts. Figure 5.8 illustrates MOS capacitor cross section.

![Figure 5.8 Cross section of a MOS capacitor](image-url)
MOS capacitor has the highest device density (≈ 11.1 fF/μm² for 130nm process). However, these types of capacitors have non-linear capacitance. In addition, these capacitors require biasing and suffer from a relatively high series resistance and have low break-down voltage. Their use is limited to high capacitance applications such as blocking capacitors on DC lines.

**Metal-Oxide-Metal and Metal-Insulator-Metal Capacitors**

The AC coupling capacitors in the signal path require capacitor with high linearity and high quality factor. Such capacitors are commonly realized with parallel plate structures such as Metal-Oxide-Metal (MOM) capacitors or Metal-Insulator-Metal (MIM) capacitors. Figure 5.9 illustrate a Metal-Oxide-Metal (MOM) parallel plate capacitor and its equivalent circuit. Total capacitance is determined by a parallel connection of three capacitors formed by four metal plates. MOM capacitors suffer from a low capacitance density which arises mainly due to large metal-to-metal spacing. Furthermore, MOM capacitors have significant parasitic capacitance to the substrate. This parasitic substrate capacitance introduces significant losses at signal coupling.

![Figure 5.9](image)

*Figure 5.9  a) Cross section of a MOM capacitor  b) equivalent circuit*
Metal-Insulator-Metal (MIM) capacitors have higher quality factor, low dielectric loss and relative high capacitance density. It has a parallel plate structure with an extra dielectric layer of reduced thickness. The MIM capacitors are usually realized in top metallization layers to reduce the parasitic capacitance to the substrate. The cross section and the equivalent circuit model of a MIM capacitor are shown in Figure 5.10.

![Figure 5.10](image)

**Figure 5.10**  a) Cross section of a MIM capacitor b) equivalent circuit

**MOS Varactors**

MOS varactors are commonly used in LC-resonators where variable capacitor is needed for frequency. A cross section of a NMOS varactor on a $p$- substrate and its small-signal equivalent circuit are illustrated in Figure 5.11.
Figure 5.11 Cross section and small signal model of NMOS varactor

The MOS varactor can be formed from a MOS transistor with drain and source terminals shorted. The bulk terminal is grounded and tuning voltage $V_{tune}$ is applied to the source-drain terminal and the voltage $V_{gate}$ is applied to the gate terminal. As a result, a variable capacitance $C_v$ is formed by the series connection of the gate oxide capacitance $C_{ox}$ and the depletion region capacitance. This capacitance is given as:

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d}$$  \hspace{1cm} (5.23)

As shown in Figure 5.12, the MOS varactors can operate in three different regions: accumulation, depletion or inversion.
Figure 5.12  Typical varactors capacitance and lumped element model

NMOS varactor is in accumulation when the negative voltage is applied to the gate resulting in the excess holes at the surface of the semiconductor. In the accumulation mode, the series resistance $R_v$ is formed by the gate resistance in series with the resistance from the accumulation layer to the substrate (well) contacts outside the device. The maximum capacitance of a varactor depends on the gate oxide capacitance $C_{ox}$.

As the gate voltage increases the flat-band situation is reached. The semiconductor beneath the gate becomes neutral and the gate charge is balanced by fixed oxide and interface charges. The flat-band voltage $V_{FB}$ is usually negative but approaches zero if the gate and well have the same doping types. Varactor operates in depletion region when the gate voltage exceeds flat-band voltage $V_{FB}$. In depletion region, holes are repelled from the surface and the negatively charged ions of fixed acceptors are repelled from the depletion region. The gate charge is balanced by more or less negative dopants, i.e. by a wider or shallower depletion region. As a result, the
capacitance in depletion region is the sum of the gate oxide $C_{ox}$ and variable depletion region capacitance $C_d$. The series resistance $R_v$ is lower than that of the accumulation mode, since the resistive path is shorter.

The device enters the inversion region when the gate voltage exceeds threshold voltage $V_{th}$. In this region of operation, the depth of the depletion region remains constant and the electron in inversion layer balances the changes in the gate charge. The varactor capacitance is determined only by the gate oxide capacitance $C_{ox}$. The resistance $R_v$ is determined by the inversion layer.

5.3.2 Inductors

Inductors are commonly used in RF circuit’s matching networks or resonant load tanks. They can be realized either with single planar layer or with multiple layers. In this work, symmetrical inductors are used for differential circuits. Symmetrical structures are preferred for their inherent low sensitivity to substrate noise. However, the layouts and modeling of symmetrical structures are more complicated. A 3D view of a symmetrical inductor is shown in Figure 5.13.

![Figure 5.13 3D Cross section of symmetrical inductor](image)
Figure 5.14 illustrate a physical π-model of the inductor. The model parameters are described as:

1. $L$: The total inductance caused by the magnetic flux density $B$ of the electromagnetic field.
2. $Rs$: The series resistance of the metal traces with finite conductivity, skin-effect and current crowding.
3. $R_{sub}$: The substrate resistance.
4. $Cp$: The lateral capacitance between the turns of the inductor.
5. $Cox$: The oxide capacitance above the substrate.
6. $C_{sub}$: The equivalent substrate capacitance.
Figure 5.15 illustrate a physical $\pi$-model of a symmetrical inductor. This model allows accurate modeling of the coil in a balanced or in a single-ended configuration. Additionally, a parameter $k$ distributes single ended Cox to each branch. The lumped component modeling does not accurately characterize inductance at high frequency or for large bandwidth. To accurately model inductance for high frequency and for large bandwidth circuits, numerical methods such as electromagnetic simulators have to be employed. The most commonly used field solver methods are:

1. *method of moments (MoM)* implemented in Agilent corp’s MOMENTUM software and this method is best suited for planar structures

2. *finite element method (FEM)* used in Ansoft corp’s HFSS software and this method is best suited for 3D structures.
5.4 IBM 8 RF CMOS Process

IBM 8 RF CMOS technology offers eight metallization layers including three levels of thick top metal layers, MIM capacitors and hyper-abrupt varactors. Additionally, the process offers transistors that can have different threshold voltages (low $V_t$, regular $V_t$ and high $V_t$). The cross section of the process is shown in Figure 5.16.

---

**Figure 5.16** Metal layer stack of IBM 8RF Process
As shown above, IBM 8RF process offers five thin copper metallization layers, two double thickness metal layers and three thick aluminum top metal layers. The silicon dioxide with dielectric constant $\varepsilon_r = 4.1$ fills the space between the metal layers. The top metal layer is covered with a layer of oxide/nitride/polyimide except for the pad openings. Three thick metal layers enable implementation of high-Q inductors.

IBM 8 RF process provides standard MIM, single MIM and dual MIM with device density of $1.35 \text{ fF/} \mu\text{m}^2$, $2.0 \text{ fF/} \mu\text{m}^2$ and $4.1 \text{ fF/} \mu\text{m}^2$ respectively. In addition, process offers n+ diffusion ($73 \Omega/ \mu\text{m}^2 +/− 15\%$) p+ polysilicon ($340 \Omega/ \mu\text{m}^2 +/− 20\%$), p-polysilicon ($1450 \Omega/ \mu\text{m}^2 +/− 25\%$) and tantalum nitride resistors ($60 \Omega/ \mu\text{m}^2 +/− 6\%$).
CHAPTER 6

MB-OFDM UWB RECEIVER IMPLEMENTATION

6.1 Introduction

The block diagram of the implemented MB-OFDM-UWB direct conversion receiver is shown in Figure 6.1.

Figure 6.1 Receiver Architecture

The receiver path consists of a single ended LNA, followed by quadrature mixers. A channel-select filter follows the IQ mixer and performs the channel selection. Then, filtered signals pass through a programmable gain array (PGA), which adjusts the gain level to avoid signal saturation at the interface of subsequent ADC. Furthermore,
LNA provides some gain control to avoid saturation in signal path when received
signal power is very high.

Following chapter presents detailed design analysis of each of the blocks in the
receiver chain shown above. Careful design tradeoffs among the various cross dependent
issues are made to create an optimal low power and cost effective design. In our design
presented here, followings are the key objectives:

1. Reliable: System shall be robust against interferences from the existing spectrum
   users.

2. Low Power: Power optimum receiver design.

3. Low Cost: Employ little or no on-chip inductors, minimum chip area and
   minimum use of off-chip components.

6.2 Low Noise Amplifier (LNA)

The LNA as the first component in the receiver signal chain sets the sensitivity of
the receiver. LNA must provided sufficient gain while creating little noise to suppress
noise contribution of the following stages. LNA interface to the outside world requires
robust electrostatic discharge (ESD) protection and input match to antenna impedance,
which is generally 50 ohms, to avoid signal reflection. Taking into account these
requirements, a careful analysis is performed to choose the right topology for this crucial
component.

6.2.1 Review of Traditional Low Noise Amplifier

The most commonly used low noise amplifiers in the RF receiver front-end are
the common-source LNA with inductive degeneration and common gate amplifier. These
amplifiers perform well in narrow-band wireless communication but are unsuitable for wide-band application without any modification. A detailed analysis of these topologies is presented here for an insight into developing broadband amplifier design.

**Common-Source LNA with Inductive Degeneration**

The common-source (CS) amplifier employs two inductors to provide a matched input impedance and a resonant load centered at the signal frequency, as shown in Figure 6.2.

![Figure 6.2 Common source amplifier with inductive degeneration](image)

For this common source amplifier, input impedance is as follows:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s$$  \hspace{1cm} (6.1)

Without introduction of degeneration inductor $L_s$, input impedance presented by the common source transistor is highly capacitive. The inductor $L_s$ synthesizes a real resistance to allow impedance match to real source resistance. Input matching requires adherence to the following relationship:
\[ R_s = \frac{g_m}{C_{gs}} L_s = \omega_r L_s \]  
(6.2)

Gate inductor \( L_g \) sets the resonance frequency of the amplifier, where resonance frequency is as follows:

\[ \omega_0 = \sqrt{\frac{1}{(L_g + L_s)C_{gs}}} \]  
(6.3)

The noise figure of the LNA can be calculated from the equivalent circuit shown in Figure 6.3. The resistor \( R_{lg} \) models the resistive loss of the inductor \( L_g \), resistor \( R_g \) the gate resistance of the NMOS transistor, \( i_d^2 \) the device channel thermal noise and \( i_g^2 \) the induced gate noise.

\[ \text{Figure 6.3} \quad \text{Small signal model for noise calculation of CS amplifier} \]

Neglecting gate to drain overlap capacitance, noise figure of the circuit is as follows [22]:

\[ F = 1 + \frac{R_l}{R_s} + \frac{R_s}{R_s} + \frac{\gamma X}{\omega_0} + \frac{\omega}{\omega_r} \]  
\[ \left( \frac{\omega_0}{\omega_r} \right) \]  
(6.4)
Where $\alpha$ is the gate noise coefficient, which equals to $\text{gm/gd}_0$, and $\gamma$ is thermal noise coefficient, which equals 2/3 for long channel device and varies from 2 to 3 in short channel device. $Q_L$ represents the quality of the input tank circuit; $\chi$ relates correlated gate noise with channel thermal noise.

$$Q_L = \frac{\omega_0 (L_S + L_g)}{R_s} = \frac{1}{\omega_0 R Sc_{gs}} \quad (6.5)$$

$$\chi = 1 + 2k_e |Q_L| \sqrt{\frac{\delta \alpha^2}{5\gamma}} + \frac{\delta \alpha^2}{5\gamma} (1 + Q_L)^2 \quad (6.6)$$

$$c = \frac{i_g i_d^*}{\sqrt{i_s^2 i_d^2}} \quad (6.7)$$

Above-mentioned equations indicates that LNA performance degrades as the operating frequency approaches the transistor’s unity gain frequency ($\omega_0$) since both noise factor ($F$) and trans-conductance ($\text{gm}$) are proportional to $\omega_0$ and $1/\omega_0$ respectively.

*Common-Gate LNA*

In the common-gate (CG) LNA, the input signal directly drives the source terminal of the transistor, as shown in Figure 6.4. Bypass capacitor at the gate terminal keeps the gate terminal at AC ground while providing high impedance DC biasing. Input matching circuit and output tank circuit can easily absorb parasitic gate-source and gate-drain capacitors. Therefore, common gate amplifier can potentially operate at high frequency.
Small signal model of the CG amplifier is shown in Figure 6.5 below.

Input impedance of CG amplifier is as follows:
\[ Z_{in} = \frac{r_{ds} + Z_L}{1 + (g_m + g_{mb})r_{ds} + r_{ds} + Z_L} \]  

(6.8)

With input impedance matched to source resistance, trans-conductance and noise factor are as follows:

\[ G_m = \frac{1}{2R_s} \]  

(6.9)

\[ F = 1 + \frac{\gamma}{\alpha} \left( 1 + \kappa \right) \left( \frac{r_{ds}}{r_{ds} + R_L} \right) \]  

(6.10)

where \( k \) is the ratio of the back-gate trans-conductance to that of MOS trans-conductance \((g_{mb}/g_m)\). With \( r_{ds} \propto I_D \), noise factor equation simplifies to:

\[ F = 1 + \frac{\gamma}{\alpha} \left( 1 + \kappa \right) \left( \frac{1}{1 + R_L \lambda I_D} \right) \]  

(6.11)

Above-mentioned equation indicates that enhancing CG LNA performance requires increase in power consumption.

6.2.2 Broadband Low Noise Amplifier

Traditional broadband LNA design techniques targets existing narrowband applications and are unsuitable for UWB applications. The most common wide bandwidth LNAs are (a) resistive shunt feedback (b) multi-section LC input filter and (c) distributed amplifier. Following sections illustrates performances of these wide band LNA performances.

1. Resistive Shunt feedback LNA:

Resistive shunt feedback LNAs employs local feedback to match input impedance of the active device to the source impedance for a wide bandwidth of operation.

For output impedance match, circuit employs an output resistor that matches the
load resistor. Fig. 6.6 below illustrates the commonly used resistive shunt feedback LNA.

![Resistive Shunt Feedback Wide-band LNA](image)

*Figure 6.6 Resistive Shunt Feedback Wide-band LNA*

Shunt feedback LNAs can provide reasonable gain and low noise performance with little area overhead since they comprise few passive and active elements and avoids area expensive inductive element. They find wide use in optical receivers. However, shunt feedback LNA has the following drawbacks:

a) **Poor high frequency performance**

Performance of shunt feedback LNA degrades at high frequency due to presence of low frequency output pole that occurs in typical LNA applications. For example, a typical interface of LNA may comprise 1 pF of load capacitance and may require 100 ohm output resistance for output impedance match. As a result, output pole of such LNA is at approximately 1.6-GHZ degrading performance of the receiver, which is required to cover entire UWB band of 3.1 GHZ to 10.6 GHZ.
b) Poor Noise Figure and linearity

In resistive shunt feedback LNA, the feedback resistor tends to be high (typically few hundred ohms) as it needs to match with source resistor (typically 50 ohms) divided by the loop gain. The high feedback resistor required for input matching degrades NF performance. Furthermore, shunt feedback LNA in CMOS implementation requires large amount of power to provide reasonable gain due to low gm of the MOS transistor. To meet linearity requirement of UWB receiver, resistive shunt feedback LNA will consume a significant amount of chip area.

2. Wide-band LNA with multiple LC sections:

Input matching circuit employs multiple LC section filter to provide input match for a wide bandwidth of operation. This type of wide-band LNA can provide high gain and low noise performance at the expense of large chip area. Fig. 6.7 below illustrates a wide-band LNA with multiple LC section input match.

*Figure 6.7* Wide-band LNA with multiple LC section input match and shunt peaking load [23].
3. Distributed LNA:

Distributed amplifier (DA) has excellent input and output impedance matching characteristics for wide bandwidth. However, DA suffers from low noise performance and high power consumption. Fig. 6.8 below illustrates a wide-band DA.

![Broadband distributed LNA](image)

*Figure 6.8* Broadband distributed LNA [24].

6.2.3 MB-OFDM UWB Low Noise Amplifier Implementation

LNA design techniques presented above are not suitable for a low cost, low power UWB receiver since they either consume large amount of power or require large die area. Careful consideration of specifications and topologies are must for finding an optimum solution. Power consumption and area overheads are the main criteria used to find the topology. Taking into consideration of these parameters, design employs the single-ended common gate (CG) LNA architecture, which provides broadband input matching while consuming lower power and die area.
Single ended CG structure provides antenna matching without the use of area expensive balun (single ended to differential converter). However, it is prone to signal corruption due to coupling of noise from substrate and crosstalk. Therefore, layout of the CG is very important for elimination of performance degradation by substrate noise coupling and crosstalk. Additionally, proposed CG structure employs a grounded inductor at the input matching circuit to resonate out the parasitic capacitance of the source terminal and protect circuit from high voltage ESD pulses by providing low impedance path to ground. CG structure uses cascode stage to increase amplifier’s stability and gain at high frequency. Additional guiding principles for good LNA performance are:

1. Inductor used in input matching and load tank must account for quality factor and DC current driving capabilities. Therefore, an accurate modeling of inductor in high frequency design is essential.

2. Transistor layout must employ multi-finger gate layout to reduce gate resistance, thereby reducing gate-induced noise. In addition, layout must include adequate substrate contacts and guard rings to reduce effective back-gate resistance.

Figure 6.9 illustrates simplified schematic of the implemented LNA.
Figure 6.9  Simplified schematic of implemented LNA

Input Matching:

Input matching network in most existing broadband CG amplifiers uses multi-stage passband network to increase the operation bandwidth. The drawbacks are increase die area due to area intensive integrated inductors and NF degradation due to low quality factor of the on-chip inductors. Proposed design takes the advantage of the feedback to provide input match. Input impedance and transfer function of LNA are as follows:

\[ Z_{in}(j\omega) = \frac{1}{g_m} + \alpha Z_{load}(j\omega) \]  \hspace{1cm} (6.12)
\[ T(j\omega) = \frac{Z_{load}(j\omega)}{Z_{in}(j\omega)} \]  

(6.13)

Where \( gm \) is the trans-conductance, \( \alpha \) is the feedback factor and \( Z_{load}(j\omega) \) is the load impedance. Feedback factor provides additional flexibility in achieving input match, which can be achieved by setting \( \frac{1}{gm} + \alpha R_t = R_s \), where \( R_s \) and \( R_t \) are the source and load tank resistance respectively. Input matching circuit achieves S11 < -12 dB for all tuning range as shown in Figure 6.10 below.

\[ \text{Figure 6.10} \hspace{1em} \text{Simulated insertion loss of LNA} \]

\[ \text{LNA Gain:} \]

Since MB-OFDM is a frequency hopping system, LNA is not required to cover the whole band. Instantaneous bandwidth of the LNA is only 528 MHz. As a result, design incorporates tuning network at the load. Load tuning circuit employs bondwire inductor for upper band since bond wire doesn’t require expensive die area and comes as
free since it is used to connect to the package itself. However, load tuning circuit at lower band employs on-chip inductor since large inductance is required at lower band. LNA uses switchable shunt resistor to broaden the bandwidth of the amplifier.

The use of bondwire inductance makes tuning load sensitive to packaging and process variation. Bondwire inductance usually varies $\pm 10\%$ from packaging to packaging due to variation of bondwire length. These variations would result in $\pm 5\%$ variation of center frequency of tuned load. However, this frequency shift results in very small drop in gain at the band edges as shown in Figure 6.11. This reduced susceptibility to variations in bondwire length and on-chip capacitance is the result of the low Q of the load tank. Furthermore, LNA achieves a minimum of 7 db attenuation of 802.11b/g and Bluetooth jammers in 2.4 GHZ band and 5 GHZ UNII band.

*LNA Gain Control, NF and Linearity:*

Proposed LNA includes current steering at the cascode (M2C) to provide gain control steps of 12 dB without disturbing input impedance match. The LNA exhibits a peak gain of 19 dB and overall 3 dB bandwidth of more than 2.4 GHz. The simulated noise figure of the LNA is lower than 4.6 dB in the whole frequency range and IIP 3 is -3.2 dBm. This LNA consumes 3 mA from a 1.2 V supply. Figure 6.12 below shows noise figure, 1dB compression point and IIP3 of the LNA.
Figure 6.11  LNA gain a) Lower Band b) Upper Band
a)

b)
As mentioned in chapter three, MB-OFDM UWB architecture easily lends itself to direct conversion because static and time-varying DC offsets can be easily removed from MB-OFDM modulation where the subcarrier around DC is not used [5], and because the wide bandwidth makes flicker noise less critical. However, direct-conversion mixer for zero-IF receiver has to fulfill several requirements. First, it must provide certain amount of gain to the receiver chain to suppress the noise contribution of the following stages. Additionally, it is preferable to optimize the noise performance of the mixer, as the low noise figure of the mixer reduces the gain requirements of the LNA. It is worth pointing out that the overall linearity of the receiver can be improved if the gain of the LNA can be reduced.

Figure 6.12 Simulated results of the LNA

6.3 RF Down-conversion Mixer

As mentioned in chapter three, MB-OFDM UWB architecture easily lends itself to direct conversion because static and time-varying DC offsets can be easily removed from MB-OFDM modulation where the subcarrier around DC is not used [5], and because the wide bandwidth makes flicker noise less critical. However, direct-conversion mixer for zero-IF receiver has to fulfill several requirements. First, it must provide certain amount of gain to the receiver chain to suppress the noise contribution of the following stages. Additionally, it is preferable to optimize the noise performance of the mixer, as the low noise figure of the mixer reduces the gain requirements of the LNA. It is worth pointing out that the overall linearity of the receiver can be improved if the gain of the LNA can be reduced.
Additionally, direct-conversion mixer has stringent IP2 and IP3 requirements. Non-linearity of trans-conductor, switch, and RF-to-LO coupling degrade the IP2 and IP3 of the down-conversion mixer [32], [33]. The switching core, which does the actual frequency translation, has to be highly symmetrical to avoid IP2 problems. Note that there are two mechanisms that can contribute to the IP2. The first mechanism is the creation of sum and difference frequencies that fall directly into the wanted RF signal band; they are translated to baseband signals by the mixer in subsequent operation. The second mechanism is the creation of difference frequency of closely spaced interferers or modulation components of a single interferer. This inter modulation product can reach the output port by RF-Output leakage in the switching core, without any frequency translation. Symmetric design of the switching core can keep this leakage at a low level improving IP2 of the mixer. In narrowband application, IP2 due to first mechanism is negligible as pre-filter is employed prior to LNA to reduce interferer power. UWB system with large bandwidth must need to address IP2 due to first mechanism making the design more challenging. However, IP3 consideration predominate IP2 in mixer under-stage since even-order distortion components in its balanced output currents will approximately cancel. Figure 6.13 illustrates architecture of quadrature single balanced down conversion mixer implemented in this project.
Figure 6.13 Single Balanced Mixer Schematic

The choice of single-balanced mixer instead of its double-balanced alternative is due to the following reasons. First, double-balanced implementation requires power consuming single-to-differential converter. Second, the double-balanced implementation generates higher noise. However, one of the drawbacks of single-balanced mixer is the presence of the local oscillator (LO) tone at the mixer output signal generated by the modulation of the biasing current. Furthermore, simple architecture shown in Figure 6.13 suffers from limited linearity.

Linearity of the mixer is very critical, as the mixer needs to deal with the amplified signals at the output of the LNA. To increase mixer linearity requirements, the implemented mixer under-stage incorporates resistive degeneration to increase dynamic range of the mixer. But, resistive degeneration negatively impacts noise figure. However, overall impact of mixer’s resistive degeneration on NF is marginal as the gain stages precede the mixer block.
Furthermore, simple architecture shown in Figure 6.13 suffers from limited gain at the high frequency as the parasitic capacitor at the source terminals of switching cores limits the commutation bandwidth. A 2-nH inductor L1 is added to tune out this capacitor, improving conversion gain, noise performance, and linearity. The gain boost is important since switching pair contribution of noise figure is non-negligible at higher frequency portion.

The proposed topology also incorporates current bleeding PMOS current source to halve the bias current commutated by switching pairs, thereby allowing these transistors to switch faster and hence inject less noise to the output [34]. Lower DC current in the switching stage saves DC headroom at mixer output and allows the load resistor to be doubled for a given a voltage headroom, raising conversion gain by 6dB. Furthermore, current bleeding improves under-stage trans-conductor linearity and noise performance by providing increased currents at the trans-conductor.

Layout of the mixer switching pairs plays an important role in IP2 performance, conversion gain and NF performance. Higher LO amplitude has positive impact on mixer gain and fast switching improves IP2 performance. However, it doesn’t eliminate negative impact of mismatch in switching pairs on IP2 performance. To reduce second-order inter-modulation products falling in the band of interest and improve IP2, switching pairs incorporate layout with interleaving fingers to increase matching. Finally, mixer implementation incorporates a low pass filter with corner frequency of 240 MHZ at the output providing substantial attenuation of LO tones. The completed schematic of the mixer is shown in Figure 6.14.
Figure 6.14 Complete Mixer Schematic

Mixer Conversion Gain:

The mixer RF stage employs a trans-conductor \( M1 \) to convert the voltage-mode RF input signal to a current:

\[
i_d(t) = G_m v_m \sin(\omega_m t) \quad (6.14)
\]

where, \( Gm \) is the trans-conductance of the RF input transistor M1. This current-mode RF signal feeds through the current switching pairs \( M2-M3 \) driven by the LO signal, which can be expressed as multiplication with square signal:

\[
i_{out}(t) = i_d(t) \text{square}(\omega_{Lo} t) \quad (6.15)
\]

This multiplication of RF signal with square function performs the frequency translation.

For example, LO signal can be written as a Fourier series:
\[ \text{square}(\omega_{LO}t) = \frac{4}{\pi} \sin(\omega_{LO}t) + \frac{4}{3\pi} \sin(3\omega_{LO}t) + \frac{4}{5\pi} \sin(5\omega_{LO}t) + \ldots \quad (6.16) \]

As a result, the output signal can be expressed as:

\[ \text{square}(\omega_{LO}t) \sin(\omega_{m}t) = \frac{1}{2} \cos\left(\frac{\omega_{m} \cdot \omega_{LO}}{2}\right) + \frac{1}{2} \cos\left(\frac{\omega_{m} + \omega_{LO}}{2}\right) \ldots (6.17) \]

where, for down-conversion operation, the first term is the desired signal and all other frequency components should be attenuated by the filter. This current-mode IF signal is then converted to the voltage at the output stage. The mixer voltage conversion gain is as follows [25]:

\[ A_v = \frac{2}{\pi} G_m R_L \quad (6.18) \]

where

\[ G_m = \frac{1}{R_s + \frac{1}{g_m}} \quad (6.19) \]

and \( g_m \) is the trans-conductance of V-I stage saturated transistor (M1).

\[ g_m = \mu_n C_ox \frac{W}{L} (V_{gs} - V_T) \quad (6.20) \]

\[ g_m = \frac{2I_D}{(V_{gs} - V_T)} \quad (6.21) \]

Therefore, increasing the width (W) of the transistor, while keeping length (L) at minimum, increases the gain. Higher overdrive voltage also increases the gain.
Mixer Input referred third order intercept (IIP3):

The linearity of the mixer trans-conductance stage is crucial to the overall performance of the mixer. A MOS transistor can be modeled with [26]

$$i_{DS} = \frac{K W}{2 L} \frac{(V_{gs} - V_T)^2}{1 + \theta(V_{gs} - V_T)}$$

(6.22)

where $\theta$ captures the effect of effect of short channel. The $IIP3$ of a down-conversion mixer can be approximated as [27]

$$V_{IIP3} = \frac{4}{\sqrt{3}} \sqrt[3]{\frac{V_{eff}(2 + \theta V_{eff})}{\theta}} \left(1 + \theta V_{eff}\right) \approx 4 \sqrt{\frac{2 V_{eff}}{3}}$$

(6.23)

where, $V_{eff} = V_{GS0} - V_T$, $V_{GS0}$ is the DC bias voltage at the gates of $M_I$ and the approximation holds if $\mu V_{eff} << 1$ [30]. The above equation shows that the $IIP3$ of mixer scales up by increasing the $V_{eff}$. Furthermore, the long channel length of input transistors improves the linearity, since $\mu$ is inversely proportional to the channel length. As the $V_{eff}$ of the input transistors $M_I$ defines the $IIP3$, the dimensions of the input transistors determine the trans-conductance of the input stage and the bias current as shown in the equation below:

$$g_m = \frac{K W}{2 L} \frac{(2 + \theta V_{eff})V_{eff}}{(1 + \theta V_{eff})^2} \approx \frac{2I_{DS}}{V_{eff}}$$

(6.24)

Mixer Noise Figure (NF):

Down-conversion mixer aliases both the desired signal and the image signal at the output. Single sideband (SSB) or double sideband (DSB) noise factor defines output noise if the mixer converts signal from both upper and lower bands. In heterodyne
receiver, which converts only one of the input RF sidebands to the IF frequency and rejects signal at the image band, the SSB noise factor is applicable. However, in a direct conversion receiver, mixer converts signals at both upper and lower bands to IF frequency. Therefore, DSB noise is applicable to direct conversion receivers.

As mentioned above, current bleeding at input trans-conductor is used to decouple the mixer gain from the supply voltage, and to reduce the bias current of the switches (ISW) lowering the flicker noise at the output. The noise factor of the mixer with current bleeding can be approximated as [28] [29]:

$$F_{DSB} = \frac{\pi^2}{8} \left( 1 + \frac{\gamma_n}{g_m R_s} + \frac{2 \gamma_n I_{DS}}{g_m^2 R_s \pi A_{LO}} + \frac{1}{g_m^2 R_s R_t} + \frac{\gamma_p g_{mp}}{g_m^2 R_s} \right) \quad (6.25)$$

where the last term denotes the channel thermal noise of bleeding transistor MP

$$\bar{i_d^2} = 4kT \gamma_p g_{mp} \Delta f$$, and $\gamma_n$ and $\gamma_p$ are the channel current noise factors of NMOS and PMOS transistors, respectively. As seen from above, the bleeding current source contributes white noise but it enables higher gain and lower noise figure without degrading the linearity.

**Mixer Simulation**

In order to achieve good accuracy, the inductor structures were simulated in electromagnetic simulator and then extracted S-parameters based files were used to model the inductors. The simulated performance of the mixer is presented in Figure 6.15. The mixer exhibits the conversion gain of 11.9 dB and noise figure of less than 15 dB in the frequency range of 4 - 250 MHz while consuming 2.5 mA from a 1.2 V supply. Noise figure of the mixer rises at frequency below 4 MHz. However, this NF degradation
is not an issue in MB-OFDM UWB systems since MB-OFDM UWB systems doesn’t carry information in the 0\textsuperscript{th} subcarrier (4 MHZ).

Figure 6.15 Mixer noise figure

Mixer reaches the 1 dB CP at the input power of -4.4 dBm and the IP3 at the input power of 3.3 dBm.
Figure 6.16 Linearity of the mixer a) 1dB compression, b) IP3
6.4 Channel Select Filter

Channel-select filter used is a fourth-order Chebyshev type with a nominal frequency of 264 MHz since zero-IF architecture used reduces nominal bandwidth of I and Q channels to 264 MHz. The filter must suppress large out-of-band interferer signals, which receive only a limited attenuation from any pre-filter placed prior to the LNA. Power levels of the interferer can be more than 50 dB higher than the sensitivity level of the wanted signal. Therefore, linearity of the filter must be maximized. The channel select filter consists of two cascaded stages, each of which is a Sallen–Key structure as shown in Fig. 6.17.

Figure 6.17 Filter first stage

It employs an op-amp in an arrangement of voltage-controlled voltage source with gain $G$. The filter employs amplifiers of unity gain amplifier with source follower to meet the slew requirement. Thus, the filter experiences 1-dB attenuation in the passband. However, filter has the maximum linearity performance.
The transfer function of the circuit is as follows [35]

\[
H(s) = \frac{V_o}{V_i} = \frac{G}{s^2 + \left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-G}{R_2 C_1}\right)s + \frac{1}{C_1 C_2 R_1 R_2}}
\]  \tag{6.26}

To realize the second-order lowpass function,

\[
F(s) = \frac{K}{s^2 + \beta s + \gamma}
\]  \tag{6.27}

it is necessary to match the coefficients of the same powers which lead to the following relationships:

\[
\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-G}{R_2 C_1} = \beta
\]  \tag{6.28}

\[
\frac{1}{C_1 C_2 R_1 R_2} = \gamma
\]  \tag{6.29}

\[
\frac{G}{C_1 C_2 R_1 R_2} = K
\]  \tag{6.30}

From the equation above, component values can be easily set. In addition, interfacing of the mixer and filter requires careful attention. With mixer gain of 10 dB, the LNA and mixer cascade tends to experience compression at the output of the mixer. To eliminate this bottleneck at the mixer output, filter provides a low impedance path reducing voltage swings at the outputs (X and Y – Figure 6.18) by 3 dB. This moves the compression bottleneck to the input of the mixer.
Figure 6.18 Mixer and filter interface

Figure 6.19 below shows simulated transfer characteristic and noise figure.

6.5 Programmable Gain Amplifier (PGA)

Like baseband filter, PGA in a UWB receiver is also wideband by usual standards. However, the linearity of the PGA is relaxed substantially as the preceding filter attenuates out-of-band signals. PGA linearity need only be large enough to handle the dynamic range of an OFDM waveform. PGA input is ac coupled to the preceding filter,
Filter Noise Figure

Figure 6.19 Filter gain and noise figure

Frequency

Noise Figure (NF)

Filter Noise Figure
which forms a high pass cut-off frequency of 5 KHZ. This removes the DC offset resulting from mismatches in differential signal path in the preceding mixer and filter. However, dynamic offset that appears as fixed pattern noise at the repetition rate of the hopping pattern passes through and must be dealt with by other means.

Figure 6.20 illustrates block diagram of variable gain stages of the receiver. To cover entire gain range required in this stage, gain is distributed between the first two stages, each with programmable gain from 6 dB to 15 dB. The third stage provides a fixed gain of 9 dB.

**Figure 6.20** Block diagram of baseband gain stage

Figure 6.21 illustrates typical programmable gain amplifier used in first two stages of baseband gain stage.
PGA circuit employs variable source degeneration resistors with fixed resistive load to provide variable gain. A major advantage of this architecture is that the amplifier can deliver both gain and attenuation. This can be easily accomplished by changing the ratio of load and degeneration resistors. Another advantage of this architecture is that gain variation by degeneration resistors doesn’t alter the bandwidth of the amplifier. As shown in the schematic, input differential pair translates input voltage to current, which is converted to differential output voltage by RL. Relationship between the generated current and input voltage is as follows:

*Figure 6.21 Schematic of PGA*
\[ i_{ac} = \frac{v_m}{R_c + \frac{2}{g_m}} \]  

(6.31)

The variable source degeneration resistor is implemented as a set of three resistors with CMOS switches which are controlled by inputs S0-S2. The degeneration resistors are switched to change the overall trans-conductance of the input stage providing the coarse gain tuning (3 dB/step). With the load resistor of 1k \( \Omega \) and degeneration resistors of 100 \( \Omega \), 190 \( \Omega \) and 290 \( \Omega \), gain steps are 15.6, 12, 9 and 6 dB.

The circuit draws 1.0 mA. A source follower buffers the output of the VGA to drive the output pads. The simulated frequency response and corresponding noise figure of the amplifier for all gain settings are presented in Figure 6.22.

6.6 Chip Layout

Proper layout of the chip plays an important role on the performance of the RF circuits. Furthermore, use of single ended amplifier at the input requires careful attention to noise coupling. In order to maximize performance of the receiver the following issues are considered regarding the floor planning and routing of the interconnections:

1. Utilize top thick metal layer for the routing of sensitive signal to reduce parasitic capacitance to ground and reduces wire resistance.
Figure 6.22  Simulated a) gain and NF of PGA
2. Minimize interconnection length between different building blocks to minimize noise coupling.

3. Provided large on-chip capacitors between the DC lines and ground to minimize supply noise feed-through.

4. Provide multiple ground pads around the die and large on-chip ground plane to ensure low impedance homogenous chip ground.

5. Reduce inductive coupling of bondwires by placing them perpendicularly

Figure 6.23 illustrates the layout of the chip and its bondwire positions. The chip occupies the area of 1000 um x 1000 um.
Figure 6.23 Layout of UWB receiver
CHAPTER 7

CONCLUSION

Ultra Wideband radio is a promising communication system topology with wide potential application in low cost wireless receiver. Unlike narrow-band wireless system, Ultra Wideband wireless system uses short time domain impulses to communicate information. The use of large bandwidth short time domain pulses allows UWB system to have low transmission power when communication distance is short. Low transmitted power allows UWB system to coexist with other existing wireless band users. Low transmit power also reduces cost of the wireless systems. However, UWB system requires novel design techniques since most existing circuit techniques and architectures target narrow-band system. Existing design techniques, if applied to UWB system design, can lead to either a heavily overdesigned receiver, which consumes too much power and die area, or an under-designed receiver, which fails to function properly in dense interference environment.

This thesis focuses on the design of robust MB-OFDM UWB receiver using low cost CMOS technology. A comprehensive analysis of receiver architecture is performed to find optimal system for low cost receiver implementation. UWB system operates in a crowded part of the spectrum. Signal belonging to other standards are potentially dangerous interferers. System design must be robust against these interferers. Our UWB system design considered the negative impacts of the following interferers:
1. Narrow in-band interferers in a UWB band such as 802.11a

1. Narrow out-of-band interferers such as Bluetooth, 802.11b/g

2. Multiple UWB interferers.

Careful considerations of these interferers lead to accurate specification IP3 and IP2 requirements of the receiver that can coexist in a hostile environment. High IP3 and IP2 requirements for UWB receiver are very challenging since design tends to be power hungry and area consuming. However, successful integration of UWB systems into consumer electronics requires UWB design to be both inexpensive and power efficient.

Considering ease of integration and lower implementation cost, direct conversion architecture is chosen. This eliminates the need for area expensive image reject filter and second oscillator circuit. However, direct conversion architecture suffers from time varying DC offset that needs to be dealt with in the baseband. Exhaustive simulation of the architecture is performed to define specifications of the system components. To further reduce system cost, low cost CMOS process is chosen and bond wire inductors are used extensively. Use of bond wire inductance requires design to be robust against large variation of the inductance. The variations of bond-wire length and on-chip capacitor can alter tuning frequency by +/- 15%. This issue is addressed by the use of on-chip tunable capacitors.

The biggest challenges in a MB-OFDM UWB receiver component design is the design of the LNA at front-end. Most designs presented in the literature consume either large die area (using multiple LC sections) or large amount of power (resistive LNAs). This thesis presents a novel UWB LNA design approach that exploits the time-frequency interleaving of MB-OFDM systems to dynamically tune the center frequency of the LNA.
Proposed LNA design avoids the use of on-chip inductors for higher bands and uses capacitive feedback for broadband input matching.

The MB-OFDM UWB receiver is designed in 0.13μm CMOS process. The receiver limits the use of area expensive inductors and any other specialized RF process, making it suitable for integration with baseband chip. The receiver integrates all building blocks including a variable-gain wideband LNA, a mixer for RF down conversion, low power channel select filter and programmable gain amplifier. The receiver meets all the specifications for a MB-OFDM UWB system covering the first nine frequency bands. The receiver consumes 240-mW from a 1.2V power supply while consuming 1 mm² of die area.

The research presented in this paper demonstrates RF front end of the UWB systems. When RF systems are integrated to the digital baseband systems, a lot of issues do arise. For example, substrate noise from baseband system can significantly degrade performance of RF front-end. This issue is more challenging to wideband systems. Integration of RF circuits with digital circuits needs to be studied in more detail.

Successful integration of UWB antenna will require reduction of antenna size, which presently consumes large area. Antenna size reduction techniques should be further investigated. Furthermore, impact of smaller antenna on the overall performance of the UWB systems needs to be investigated.
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