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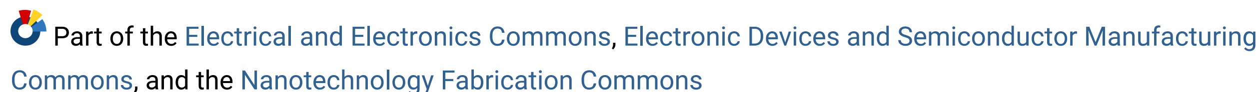
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Investigation of Nanoporous Thin-Film Alumina Templates

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This paper presents the results of a systematic study of the fabrication of thin-film alumina templates on silicon and other substrates. Such templates are of significant interest for the low-cost implementation of semiconductor and metal nanostructure arrays. In addition, thin-film alumina templates on silicon have the potential for nanostructure integration with silicon electronics. Formation of thin-film alumina templates on silicon substrates was investigated under different fabrication conditions, and the dependence of pore morphology and pore formation rate on process parameters was evaluated. In addition, process conditions for improved pore size distribution and periodicity were determined. The template/silicon interface, important for nanostructure integration on silicon, was investigated using capacitance-voltage measurements and electron microscopy, and was found to be of good device quality. Formation of thin-film alumina templates on nonsilicon substrates such as glass, indium-tin-oxide-coated glass, and silicon carbide was also investigated.
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Anodized alumina templates have received significant attention for the low-cost fabrication of semiconductor and metal nanostructure arrays.[1-3] This material system uses natural self-organization for the creation of periodic arrays of nanoscale structures. The underlying principle is that when aluminum is anodized in a suitable acidic electrolyte under controlled conditions, it oxidizes to form a hydrated aluminum oxide (alumina) containing a two-dimensional hexagonal array of cylindrical pores as shown in Fig. 1. This material was first characterized by Keller *et al.*[4] as an array of columnar hexagonal cells, each containing a pore normal to the substrate surface. The pore diameter and the interpore spacing depend on the anodization conditions such as electrolyte pH, type of acid, anodization current/voltage, electrolyte temperature, and the substrate parameters. The pore diameter can be varied between 4 nm and hundreds of nanometers and the pores can be several micrometers deep.[5-8] Due to the excellent periodicity of the pores and the ability to control the pore diameters, such anodized alumina films can be used as templates for the fabrication of periodic arrays of nanostructures. Because alumina (Al_2O_3) is electrically insulating ($10^{18}\ \Omega$ cm resistivity), optically transparent over a wide spectral range, and chemically robust, it is an ideal embedding material for optical and electronic devices.[1] The alumina templates can be used to synthesize a variety of metal and semiconductor nanostructures,[9] as well as masks for the processing of semiconductor substrates.[10] In addition, the template can be used as a mask for pattern transfer to create periodic arrays of pores on a substrate. In summary, this technology allows economic fabrication of large periodic arrays of nanostructures that allow (*i*) the size and composition of the nanostructures to be varied, (*ii*) encapsulation of nanostructures in a rugged host material, (*iii*) flexibility to use a variety of substrate materials, and (*iv*) compatibility with standard silicon fabrication technique.

While most of the work in this field has focused on bulk aluminum, the use of a bulk aluminum substrate precludes most photonic and electronic applications due to the opaque nature of the unconverted aluminum and the inability to readily integrate the nanostructure arrays with other device technologies. Therefore, direct fabrication of the template on the desired substrate is preferred, and thin-film alumina templates are of particular importance for device applications. In addition, thin-film templates formed on silicon substrates are of special interest due to their potential for nanostructure integration on silicon. This paper presents a systematic study of the formation of thin-film alumina templates on silicon and nonsilicon substrates. Thin-film alumina templates were fabricated under different processing conditions, and the dependences of pore morphology and pore formation rate on process parameters were evaluated. In addition, the template/silicon interface, which is important for nanostructure integration on silicon, was investigated using capacitance-voltage measurements and electron microscopy.

Experimental

The alumina template fabrication technique is flexible regarding the choice of substrates, and any arbitrary substrate can be used for formation of the thin-film alumina templates. While most of our research has been based on silicon substrates, we have also investigated the formation of thin-film alumina templates on nonsilicon substrates such as glass, indium-tin-oxide (ITO)-coated glass, and silicon carbide (SiC) substrates. The following sections detail the results of our investigations.

Thin-film alumina templates on silicon substrates.— Fabrication procedure.—As an example of using silicon substrates, p-type ⟨100⟩ 0.1-0.3 Ω cm silicon wafers were first cleaned using a standard technique and etched in a 1% hydrofluoric acid solution to remove any native oxide. Next, a 0.5 μm thick aluminum layer was deposited on the back of the wafers and annealed at 450°C for 30 min to form a good electrical contact. Following this, an aluminum layer (0.1-0.5 μm thick) was deposited by either sputtering or electron-beam evaporation. In most cases, the samples were then annealed at 400°C for 30 min to ensure good adhesion. The top aluminum layers were then anodized in 20% sulfuric or 20% oxalic acid under constant voltage or constant-current conditions. Anodization in sulfuric acid creates templates with smaller pore diameters compared to anodization in oxalic acid under the same conditions. Constant-current anodizations were performed at current densities ranging between 10 and 70 mA/cm^2, and constant voltage anodizations were carried out at voltages ranging between 10 and 40 V. The acid solution was circulated using a pump and chilled using a chiller to prevent heat buildup at the aluminum/electrolyte interface. To investigate the effect of electrolyte temperature on template properties, anodizations were performed at different electrolyte temperatures. The anodization process was monitored by observing the voltage-time characteristics for constant-current anodizations, and current-time characteristics for constant-voltage anodizations.

Results and Discussion

Figure 2 shows a typical voltage-time characteristic for constant-current anodization in sulfuric acid for an aluminum thin film on a silicon substrate. The voltage-time characteristic provides insight into the anodization process as explained later. While the pore formation mechanism during anodization is not yet fully understood, it is believed to take place in the following steps. During the first 3-5 s of anodization, a thin, nonporous film of alumina (Al_2O_3) called the barrier layer is formed on top of the aluminum film. As anodization is continued, an array of pores develops on the barrier layer, whose diameters increase until reaching a final dimension determined by the anodization conditions. Once the final diameter is

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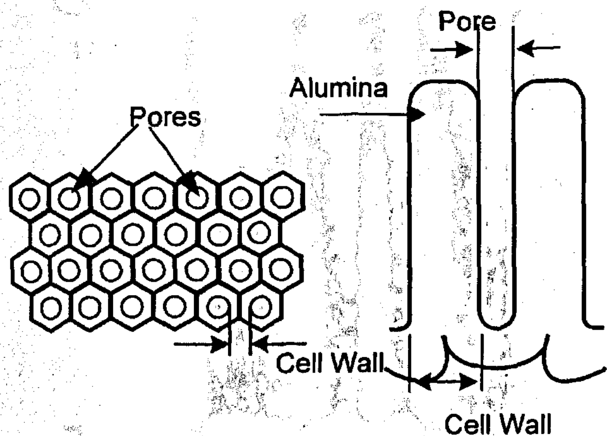


Figure 1. Top and cross-sectional views (schematic) of hexagonal array of pores formed in porous alumina template.

reached, the pore diameter does not increase any further; the pore depths increase at a rate proportional to the anodization current. For constant-current anodization, the potential across the anode and cathode is proportional to the device resistance. Thus, the potential increases during the first 3-5 s when the high-resistance barrier layer is formed. Next, as the pores start to develop, the potential decreases until the final pore diameter is reached, after which the potential remains constant as the pores propagate. When the pores reach the substrate, the potential-time characteristic shows a sharp rise in the voltage. This sharp rise is believed to be due to oxidation of the silicon surface and is discussed in a later section.

The potential-time characteristic, shown in Fig. 2, allows precise determination of the pore propagation rate from the known values of aluminum layer thickness and pore propagation time. Figure 3 shows the results of a systematic study of the pore propagation rate calculated from the potential-time curves for a number of samples anodized under different conditions. The data shown in Fig. 3 are for two different aluminum film thicknesses anodized at two different electrolyte temperatures, as well as for an unannealed aluminum thin film. Figure 3 shows that the pore propagation rate increases approximately linearly with the anodization current density, which is to be expected. It is observed that the pore propagation rate is insensitive to the electrolyte temperature. Also, the pore propagation rates for annealed and unannealed samples do not show any noticeable differences. It may also be noted that the pore propagation rate shows small sample-to-sample spread at lower anodization current densities; however, the spread increases at higher current densities. This may be due to increased heat generation at higher current densities. From voltage-time characteristics of the samples, we also calculated (a) the barrier layer formation time and (b) the pore formation time, as a function of current density; the results are shown in Fig. 4a and b, respectively. It can be seen that both parameters decrease exponentially with the anodization current density. This exponential dependence can be explained using a simple ion-concentration-limited electrochemical reaction model.

In Fig. 2, the voltage-time characteristic shows a sharp rise corresponding to the pores reaching the silicon substrate. We believe

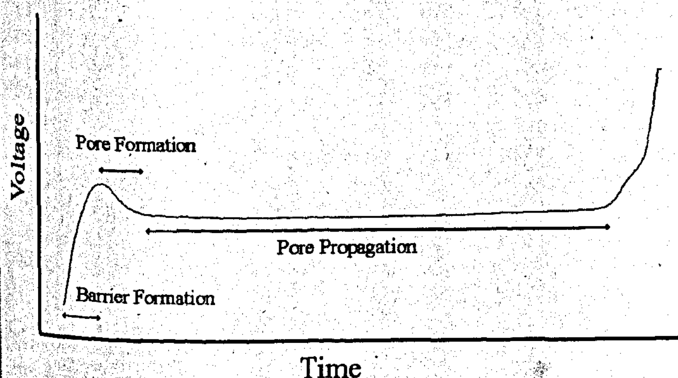


Figure 2. Typical experimental voltage-time characteristic during constant-current anodization of aluminum thin film on silicon showing barrier layer formation, pore initiation, pore propagation, and contact with substrate. The anodization time varied between 60 s and 2 min, and the sharp rise in voltage was observed at around 15 V.

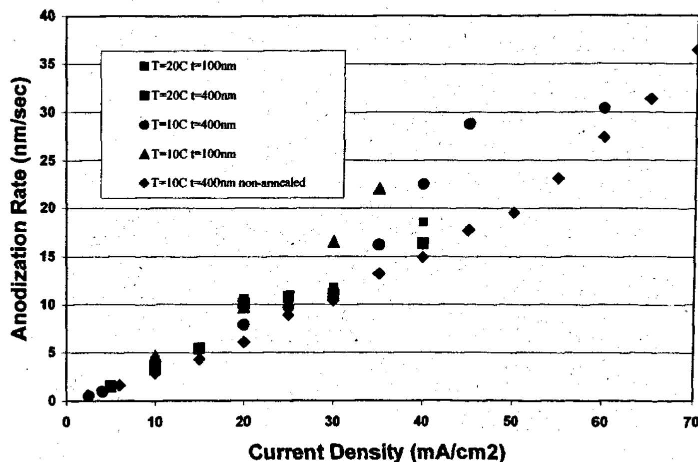
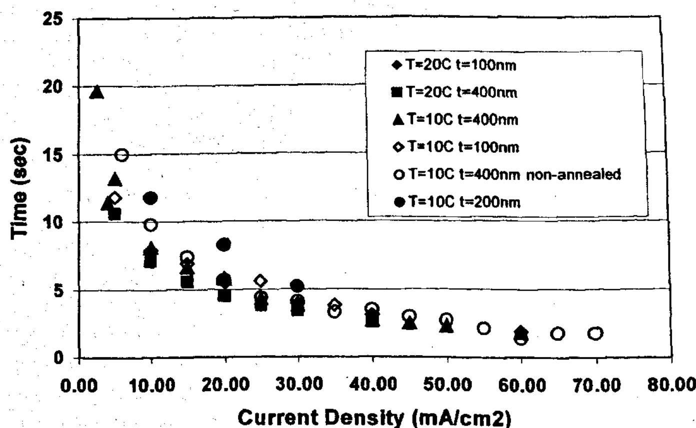


Figure 3. Experimentally determined pore propagation rate (anodization rate) as a function of anodization current density for aluminum film thickness (t) of 100 and 400 nm anodized at different electrolyte temperatures (T).



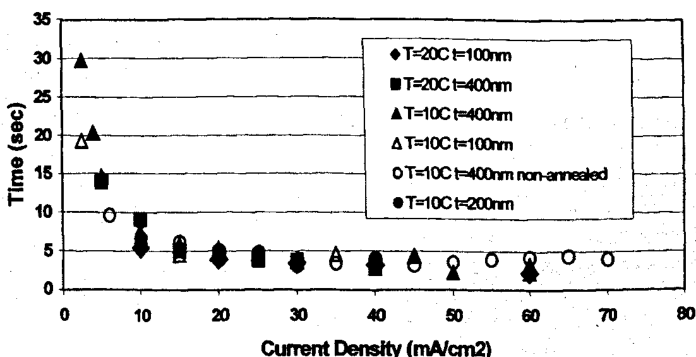


Figure 4. (a) Barrier layer formation time and (b) pore formation time as a function of anodization current density for a variety of thin-film and anodization parameters.

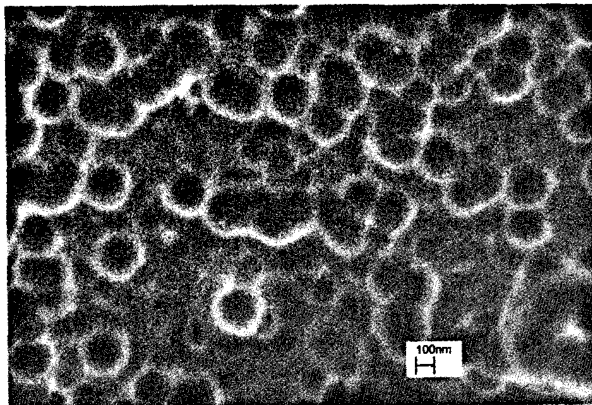


Figure 5. FE-SEM image of the silicon surface after removal of the alumina template. The circular islands are oxidized silicon formed through the pores.

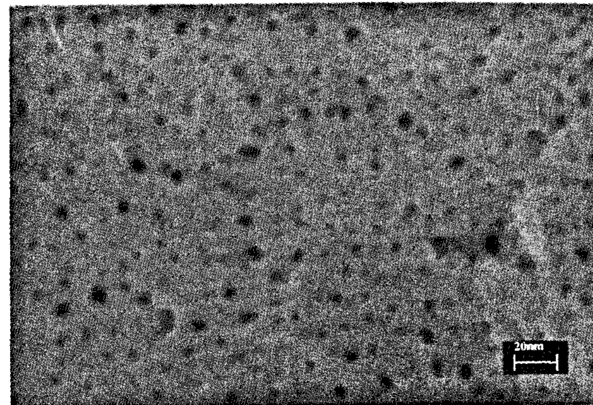


Figure 7. FE-SEM image of alumina template formed by the anodization of a sputter-deposited aluminum thin film on silicon.

that the sharp rise in the voltage-time characteristic is due to the following reason. After the aluminum layer is exhausted, if the anodization process is still continued, the electrolyte first etches the barrier layer and then oxidizes the surface of the silicon. To verify this, we removed the alumina template from the silicon substrate by etching in a chromic acid solution, and then inspected the surface under a scanning electron microscope (SEM). Figure 5 shows the field-emission (FE) SEM picture of the surface of the silicon substrate after the alumina template was removed. It may be seen from Fig. 5 that the complete surface is covered with oxidized silicon; the circular features are thicker islands of oxide at the locations of the alumina pores. By using angle-dependent imaging, it was confirmed that the circular features were islands and not pits. We believe that the silicon surface under the pores got oxidized first, after which the oxidation process spread laterally, which is the reason why the circular islands are larger than the pore dimensions. These results suggest that special care needs to be taken during the anodization of aluminum thin films on silicon substrates; the anodization process should be stopped as soon as the potential starts to increase. Another solution is to incorporate a protective layer of metal, such as platinum or gold, between the aluminum layer and the silicon substrate.

Capacitance-voltage characterization of the template/silicon interface.—The alumina templates on silicon hold significant promise for the integration of nanostructures with silicon electronic devices. For such integration, the alumina/silicon interface plays an important role, which we characterized using capacitance-voltage (C-V) measurements. C-V measurement is a widely accepted means of testing metal insulator semiconductor (MIS) capacitor samples and for determining device parameters such as carrier density, Fermi level, flatband voltage, and threshold voltage. Because anodized alumina is an insulator, C-V characterization could be used to characterize the templates as well as the template/silicon interface. Toward this goal, a number of aluminum/alumina/P-Si MIS capacitors were fabricated by first anodizing a p-type silicon wafer followed by the deposition of a number of aluminum contacts, each 1.59 mm diam, through a shadow mask. Special care was taken during anodization to avoid oxidation of the silicon surface as described before. C-V measurements were performed at a frequency of 1.0 MHz. The bias

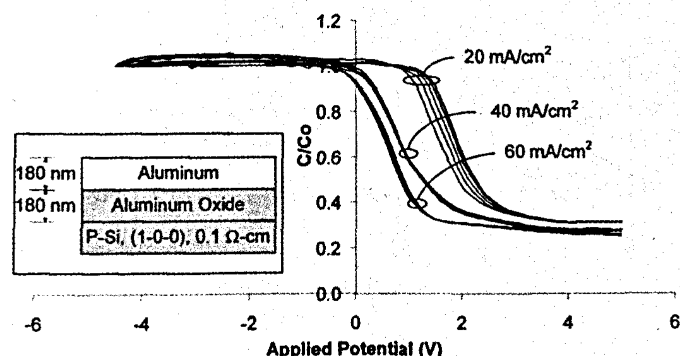
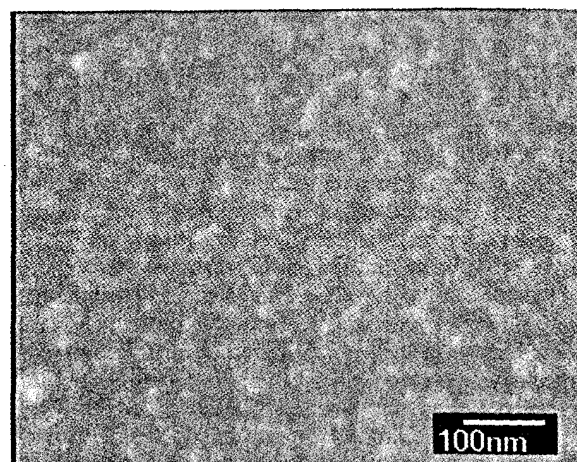
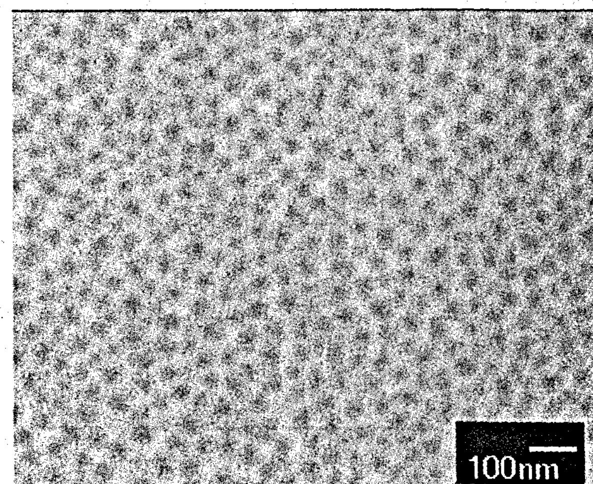


Figure 6. C-V characteristics of alumina templates formed on silicon substrates. The inset shows the devices used in the experiments.



(a)



(b)

Figure 8. FE-SEM images of (a) electron-beam-evaporated aluminum thin film on silicon and (b) template formed by the anodization of film in (a).

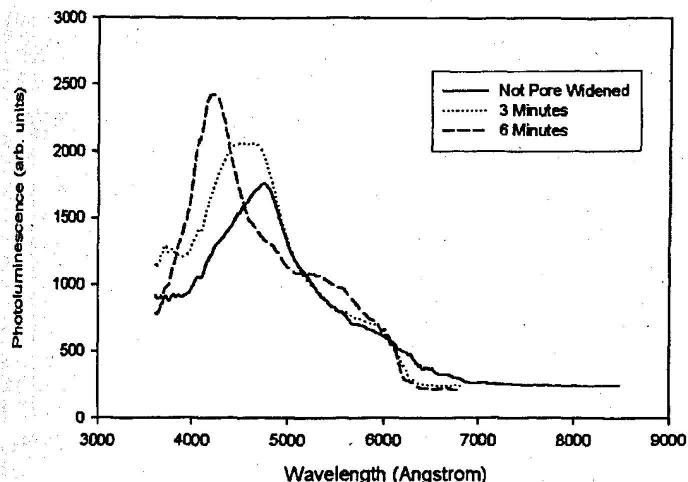


Figure 9. PL spectra from alumina templates that were not pore widened, and pore widened for 3 and 6 min. Laser excitation wavelength 325 nm; $T = 5$ K.

voltage was varied from −5 to +5 V dc, using a HP 4140A dc voltage source, controlled by Lab*VIEW* software. This voltage range was selected to avoid excessive leakage currents. The C-V characteristics for the samples are summarized in Fig. 6, which also shows the capacitors used in the experiments.

From Fig. 6, the C-V characteristics are very similar to that of typical C-V characteristics observed in metal oxide silicon (MOS) capacitors fabricated on p-type substrates. For negative bias voltages, the capacitance remains constant at C_0 (the accumulation capacitance), then decreases with positive voltage as the depletion layer forms, and then becomes constant again at C_i (the inversion capacitance). The data in Fig. 6 were normalized to C_0. The results are encouraging because they suggest that the template/silicon interface is of good device quality. Note from Fig. 6 that the threshold voltage (the bias voltage at which the capacitance starts decreasing) is close to zero for samples that were anodized at 40 and 60 mA/cm^2, and is close to 1.5 V for the samples anodized at 20 mA/cm^2. We are investigating this further and the results will be presented in a future article. It is also encouraging to note the small sample-to-sample variation in the C-V data, suggesting good uniformity of the alumina layer on silicon. The C-V measurements confirm that the alumina/silicon interface is of good device quality with the potential for nanostructure integration with silicon electronics.

Sputtered vs. vapor-deposited aluminum films.—The pore geometry and configuration in the template are expected to be influenced by the morphology of the aluminum thin film, and thus by the method of its deposition. Because sputtering is the preferred method of metallization in the integrated circuit (IC) industry, and because one of our targeted applications is nanostructured solar cells where cost is a critical factor, we have extensively investigated template formation on sputtered aluminum films. However, we also investigated template formation on electron-beam evaporated aluminum films to compare the pore morphologies. In some cases the films were annealed for improved adhesion to the silicon substrates. While annealed films did show improved adhesion, we did not notice any difference in terms of pore morphology and pore size distribution. Thus, the following discussion involves only unannealed aluminum films.

Figure 7 shows the FE-SEM image of a typical alumina template formed on a sputter-deposited aluminum thin film, which shows pronounced grain structures. The pore morphology on the grain boundary is different from that within the grains. In addition, the pores formed on the grain boundaries show better pore size uniformity and periodicity than those formed within the body of the grains. While such pore size variations are preferred for some applications such as nanostructured solar cells, the majority of applications require better pore size uniformity and periodicity. From Fig. 7 it appears that the pore size uniformity and periodicity can be greatly improved by reducing the grain size. Toward this goal, we created alumina templates by anodizing thin films of aluminum deposited by electron-beam evaporation. Figure 8a shows the FE-SEM image of an electron-beam-evaporated aluminum thin film. The film thickness is 500 nm and the deposition rate was 0.5 nm/s. As expected, the grain size for the electron-beam-evaporated aluminum is much smaller compared to that of the sputtered films. Figure 8b shows the FE-SEM image of a typical anodized alumina template formed on an electron-beam-evaporated aluminum film. The pore size uniformity and pore regularity are much better for the electron-beam-evaporated films compared to sputter-deposited films. The pore size distribution and periodicity can be further improved by a two-step anodization process that is described later.

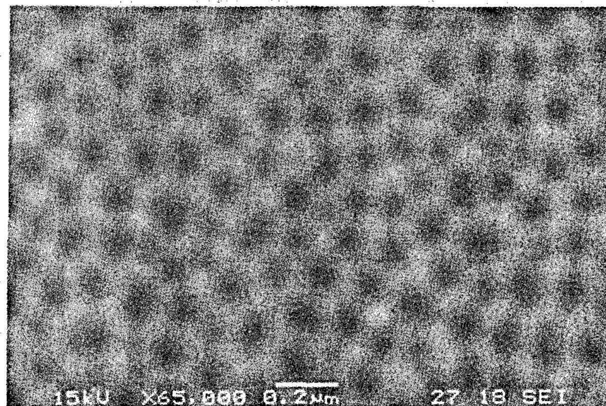


Figure 10. FE-SEM image of alumina template formed by two-stage anodization process showing good pore size uniformity and pore periodicity.

Pore widening.—A pore-widening step is often performed after the anodization step on anodized alumina by immersing it in a 5% solution of phosphoric acid for 3-5 min. The purpose of pore widening is to remove any remaining barrier layer (alumina) at the alumina/silicon interface, as well as to remove impurity ions left over from the anodization process. The pore-widening step removes a thin layer of the alumina, thus widening the pores to some degree. For thin-film templates, we perform the pore-widening step primarily as a "clean-up" step. To investigate this further, we carried out photoluminescence (PL) measurements on alumina templates that were pore widened for 3 and 6 min and compared them with an unwidened sample. The results are shown in Fig. 9. The PL measurements were performed at 5 K with a laser excitation wavelength of 325 nm. Figure 9 shows that the PL intensity increases as well as undergoes a blue shift with increased pore-widening time. We believe that the shift in the PL spectra indicates that the pore-widening process removes some of the impurities; however, it also introduces some new impurities on the template. We are currently pursuing this further to identify the specific chemical species present in the template pores.

Multistep anodization.—In recent years, for bulk aluminum, nearly perfect densely packed hexagonal pore structure has been reported by a two-step anodization process.[11-13] The bulk aluminum substrate is first anodized for an extended period of time to stabilize the pore propagation process. The alumina layer is then etched away, leaving behind "footprints" that act as seeds for pore initiation for the following anodization step. This two-step anodization process significantly increases the pore periodicity. The number of "anodization/etch" steps can also be increased to further improve the pore periodicity. This multistep anodization process typically involves tens of micrometers of aluminum. While this is not a problem for bulk aluminum substrates, it is a challenging task for thin aluminum films which are typically less than 0.5 μm thick. We have applied the multistep anodization technique on thin-film aluminum

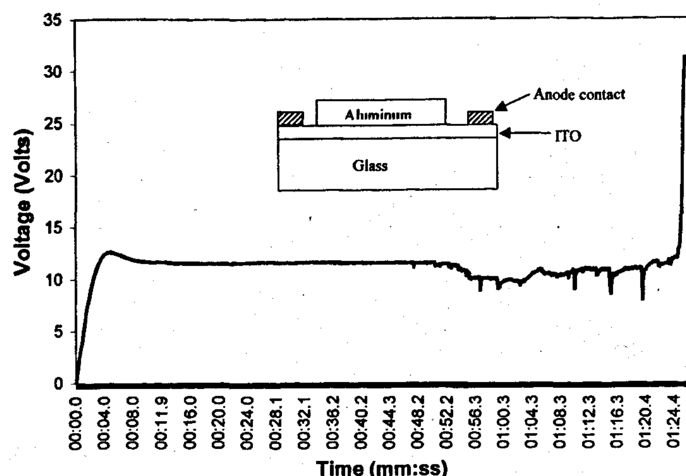


Figure 11. Voltage-time characteristic for constant-current anodization of aluminum thin film deposited on ITO-coated glass substrate. The inset shows the electrical contact configuration used in the experiment.

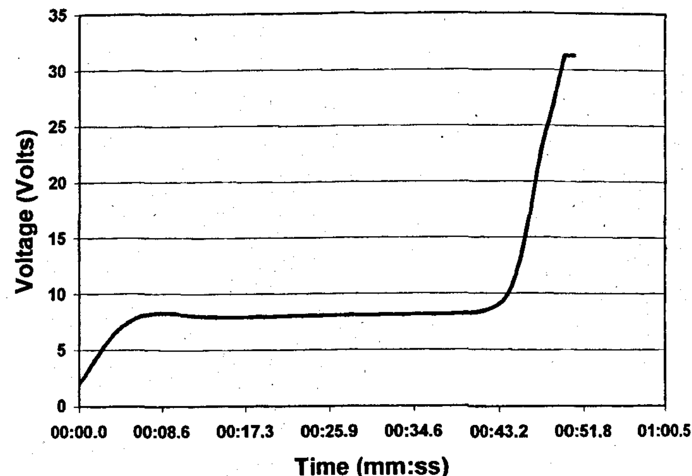


Figure 12. Voltage-time characteristic for constant-current anodization of aluminum thin film deposited on silicon carbide substrate.

on silicon substrates and were quite successful in achieving a high degree of pore periodicity. The details of the experiments together with results are presented.

p-Type silicon wafers with ⟨100⟩ orientation were used for these experiments. Silicon wafers, cleaned by standard techniques, were deposited with 0.25 μm aluminum on the back followed by annealing to form a good ohmic contact. Next, around 0.5 μm of pure aluminum was deposited on the top of the wafer using electron-beam evaporation. The top aluminum layer was then anodized in 20% oxalic acid solution using the two-step anodization process. Oxalic acid was used in order to create larger pore diameters for the ease of imaging. In the first step, around 0.25 μm aluminum was anodized and was then completely removed using a chromic acid solution. The wafer was then anodized again until the potential started to rise, indicating that the pores had reached the silicon surface. The anodization current density was varied between 5 and 70 mA/cm^2. Figure 10 shows a typical sample created at 40 mA/cm^2 current density. It may be seen from Fig. 10 that the two-step anodization process significantly increases the pore periodicity and pore size distribution.

Nonsilicon substrates.—One of the advantages of the template-based fabrication technique is that it is versatile regarding the choice of substrates. We have formed alumina templates on glass, ITO-coated glass, and SiC substrates. One of the challenges of using a nonconducting substrate is the formation of the anode contact. For SiC substrates, even though the resistivity was quite high, we could use an ohmic contact on the back of the substrate for anodization. For glass and ITO-coated glass substrates, the anodic contact could not be taken from the back, and the configuration shown in the inset of Fig. 11 was used. The potential-time curve for the constant-current anodization of aluminum deposited on ITO-coated glass is shown in Fig. 11. Figure 12 shows the voltage-time characteristics for the anodization of an aluminum thin film deposited on a SiC substrate. The voltage-time characteristics in Fig. 11 and 12 are similar to that for aluminum deposited on a silicon substrate. We believe that the rise in the voltage-time curve at the end of anodization is due to the electrochemical oxidation of SiC and ITO. Pore morphology and configuration in alumina templates formed on SiC and ITO substrates were found to be similar to that on silicon substrates. The results confirm the flexibility of the above-described fabrication technique regarding the choice of substrate.

Conclusions

The results of a systematic study of the creation of thin-film alumina templates on silicon substrates are presented. From voltage-time characteristics monitored during the anodization process, pore propagation rates were determined for a variety of metallization and anodization conditions. The pore propagation rate increased linearly with the anodization current density but was found to be insensitive to the metallization process and the electrolyte temperature. The barrier layer formation time and the pore formation time to decreased exponentially with the anodization current density. The sharp rise observed in the voltage-time characteristic during constant-current anodization is attributed to the pores contacting and the electrolyte oxidizing the silicon surface. This suggests that special care must be taken to stop the anodization at the onset of potential increase. C-V measurements performed on the alumina templates show that the template/silicon interface is of high device quality, which is significant for the integration of nanostructures with silicon electronic devices. It was observed that vapor deposition of aluminum thin films produces templates with increased pore periodicity and pore size distribution. Also, the two-step anodization process, commonly used for bulk aluminum, can be used to further improve the pore size distribution and pore periodicity for thin-film alumina templates. Thin-film alumina templates were also created successfully on a variety of nonsilicon substrates including glass, ITO-coated glass, and SiC, which is important for the creation of nanostructure devices on various of substrates including glass and plastic.

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