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Leakage gate current in a heterostructure field effect transistor

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LEAKAGE GATE CURRENT IN A HETEROSTRUCTURE FIELD EFFECT TRANSISTOR

by

Amit R. Mahajan

Bachelor of Engineering
University of Bombay, Mumbai, India
1995

A thesis submitted in partial fulfillment of the requirements for the

Master of Science Degree
Department of Electrical and Computer Engineering
Howard R. Hughes College of Engineering

Graduate College
University of Nevada, Las Vegas
August 1999

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Thesis Approval
The Graduate College
University of Nevada, Las Vegas

July, 20199

The Thesis prepared by

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Entitled

Leakage Gate Current In A Heterostructure Field Effect Transistor

is approved in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering

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ABSTRACT

Leakage Gate Current in a Heterostructure Field Effect Transistor

by

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A theoretical formulation for the leakage gate current in a heterostructure insulated-gate field effect transistor (HIGFET) is presented. Three important components of the leakage gate current, namely 2-D tunneling, 3-D tunneling and thermionic emission current, are considered. The conduction band edge profile of the HIGFET is obtained by a self consistent solution to the Poisson and Schroedinger equations. The transmission coefficient for 2-D and 3-D tunneling currents is obtained by solving the Schroedinger equation.

The leakage gate currents are obtained as a function of the gate voltage for the AlInAs/GaInAs and AlGaAs/GaAs based HIGFET structures. For the AlInAs/GaInAs system, the calculated leakage currents are within a factor of 10 of the experimental values for most of the voltage range of study. This is more accurate than the results obtained in earlier literature, where the currents are off by more than a factor of 100 for most of the voltage range. For the AlGaAs/GaAs system, the qualitative behaviour of the results are good, however, the calculated currents are off by about a
factor of 1000 for most gate voltages. The reasons for this discrepancy are discussed.
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ACKNOWLEDGMENTS

I am very much grateful to Dr. Rama Venkat for his constant support and invaluable guidance throughout the course of this study. Sincere thanks are due to Dr. Peter Stubberud, Dr. Shahram Latifi and Dr. Laxmi Gewali for serving on my thesis committee.

Finally, I would like to thank my family for their perennial support and encouragement.
CHAPTER 1

INTRODUCTION

1.1 Benefits of heterostructure semiconductor devices

In a conventional semiconductor device only one type of semiconductor is used throughout and rectification of current is achieved by creating a junction within the structure by doping. This type of device is termed a homostructure. In contrast, if more than one semiconductor material is used to form a junction, then the device is called a heterostructure device. The discontinuity of the conduction and valence energy band edges at the interface between dissimilar materials forms a potential barrier. In a heterostructure field effect transistor (HFET), a wide bandgap semiconductor separates the gate electrode from the conducting channel which is usually a narrow bandgap semiconductor. The cross section of a conventional HFET is illustrated in Figure 1.1.

Typically the various layers of the HFET are fabricated by molecular beam epitaxy, which allows for precise thickness control and interface smoothness, and the

![Figure 1.1: A schematic diagram illustrating the cross section of a conventional HFET](image)
source and drain contacts are ion implanted. Above the threshold, a two-dimensional electron gas (2DEG) forms at the heterointerface between the wide bandgap semiconductor layer and the narrow bandgap semiconductor. The thickness of this channel is typically only 100 Å which is much smaller than the deBroglie wavelength of the electron. Therefore, the electron energies are quantized in a two-dimensional system at the heterointerface, and hence, the channel electrons of the HFET form a two-dimensional electron gas (2DEG). The physical separation of the electrons from the donors (impurities) reduces the ionized impurity scattering. This increases the mobility as well as effective velocity of electrons under the influence of an electric field, which in turn, results in a dramatic enhancement in the device current and transconductance. Additionally, due to very little impurity scattering, the parasitic resistances are low and the transconductance is high and thus HFETs demonstrate impressive microwave performance [1, 2].

1.2 Heterostructure insulated gate field effect transistor (HIGFET)

A heterostructure insulated gate field effect transistor (HIGFET) is similar to the conventional HFET (Figure 1.1) except that the epitaxial layer structure is undoped in a HIGFET. Since the AlGaAs layer is undoped, there is no trapping behaviour at the interface between AlGaAs and GaAs and hence the mobility of the electrons in the channel is higher. Additionally, since the layers are undoped, the threshold voltage is just dependent on the Schottky barrier height, $\phi_s$, and the conduction band edge discontinuity, $\Delta E_c$, at the interface which in turn results in uniform threshold voltage value; a highly desirable property in IC applications. Complementary HIGFETs, which combine both n-channel and p-channel devices on the same wafer, have demonstrated low-power, high-speed operation [3, 4, 6, 7, 8, 9, 10, 11]. HIGFETs using AlGaAs/GaAs heterostructure system and AllnAs/GalnAs heterostructure sys-
tern have found use in digital integrated circuits due to the above mentioned excellent properties.

1.3 Material systems for HFETs

GaAs and closely related compounds such as GaInAs and AlGaAs grown on InP substrates are the main stream of compound semiconductor electronics. Compound semiconductors using GaAs and other related compounds are less developed as compared to silicon (Si). However, there are certain incentives for using GaAs over Si. GaAs and related compounds are capable of operating at higher speeds and lower power than Si. Since GaAs is a direct gap semiconductor it is suitable for opto-electronic device applications. Other advantages of GaAs include a high low-field electron mobility that contributes to smaller parasitic resistances and a higher device speed and a high peak velocity that leads to higher speed and operating frequencies in short-channel devices. One of the important features for fabricating heterostructures is that the materials in the heterostructure should be lattice matched. The AlAs-GaAs system is one of the only two cases where related semiconductors share virtually the same lattice constant.

Another important heterostructure system is the AlInAs/GaInAs system lattice matched to the InP substrate. The AlInAs/GaInAs system offers certain advantages over the AlGaAs/GaAs system. The most important advantage is the higher conduction band discontinuity, $\Delta E_c$, as compared to the AlGaAs/GaAs system. $\Delta E_c$ has been determined to be about 0.5 V for AlInAs/GaInAs system as compared to about 0.25 V in the case of AlGaAs/GaAs system. The higher $\Delta E_c$ in case of AlInAs/GaInAs system leads to higher 2-D charge concentration in the channel which in turn leads to a higher transconductance. Other benefits of the AlInAs/GaInAs include higher mobility and higher peak velocity that leads to higher operating fre-
1.4 Leakage gate current

The gate current in HIGFETs and other HFET devices limits the maximum gate voltage swing and the maximum transconductance and, as a consequence, the noise margin of digital circuits and increases the static power dissipation. The gate current is also dominant in the hot-electron regime when a HIGFET exhibits a negative differential resistance caused by the increase in the gate current with the drain-to-source voltage [31]. Thus, the gate current has become one of the important parameter characterizing the quality of a HFET.

There are several possible sources of the leakage gate current. Some of the important sources are the decay of 2-D charge in the conduction channel by tunneling into the wide bandgap material, decay of 3-D charge in the narrow bandgap material by tunneling into the wide bandgap material and thermionic emission over the Schottky barrier between the wide bandgap and narrow bandgap material. The contribution due to the various components mentioned above depends on the physical and material parameters of the heterostructure system and the externally applied gate voltage, $V_g$. Some of the parameters that influence the gate current are the conduction band discontinuity, $\Delta E_c$, between the wide bandgap and the narrow bandgap material and the thickness of the wide bandgap material. Higher the $\Delta E_c$, smaller is the leakage gate current. Larger the thickness of the wide bandgap material, smaller is the leakage gate current. Higher the $V_g$, larger is the leakage gate current.

To reduce the leakage gate current, a heterostructure system with a high $\Delta E_c$ should be used and the thickness of the wide bandgap material should be increased. However, increasing the thickness has an adverse effect on the transconductance of an HFET. A very thick layer of wide bandgap material will reduce the 2-D charge
concentration in the conduction channel and thus result in a lower transconductance. Hence, an optimum thickness is used for the wide bandgap material.

1.5 Overview of the thesis

A detailed literature survey on HFETs is presented in Chapter 2. The various physical components of the leakage gate current in a HIGFET and theoretical approaches to computing these components in terms of the device parameters and the applied gate voltage along with the required numerical procedures is presented in Chapter 3. Results are presented and discussed for two different HIGFET systems in Chapter 4. Conclusion along with recommendation for future work are given in Chapter 5.
CHAPTER 2

LITERATURE SURVEY

2.1 Introduction

This chapter provides a short description of device history, structure and operation of the HFETs. Some of the relevant work, both experimental and theoretical performed to date on HFET systems are summarized and discussed in this chapter. Additionally various models proposed to characterize the leakage gate current in a HIGFET are discussed in this chapter.

2.2 History

The initial concept of accumulation of charge at a heterojunction interface and it's potential for devices was introduced in the late 1960s [26]. The enhanced mobility in AlGaAs-GaAs heterostructure was first demonstrated by Dingle et al. [27] in 1978. Stormer et al. [28] reported a similar effect using a single AlGaAs-GaAs heterojunction in 1979. The first field effect transistor based on this effect was developed by Mimura et.al. [29] in 1980, and later by Delagebeaudeuf et.al. [30] in the same year. This FET was referred to as modulation-doped field-effect transistor (MODFET). In literature, devices based on the modulation doping principle are referred to by various acronyms like high electron mobility transistor (HEMT), two-dimensional electron gas transistor (TEGFET) and selectively doped heterostructure transistor (SDHT). All these devices belong to a more general family referred to as heterostructure field effect transistors or HFETs.
2.3 Structure and operation

The majority of work in HFETs has been on n-channel devices in the AlGaAs/GaAs material system. The structure of a typical HFET is as follows. An intrinsic layer of GaAs about 1 \( \mu m \) thick is first deposited on a semi-insulating GaAs substrate followed by a “spacer” layer of 30-60 \( \AA \) of intrinsic AlGaAs. The purpose of the AlGaAs “spacer” layer is to ensure the separation of the channel from the doped AlGaAs region. This ensures high carrier mobility in the channel due to the exclusion of ionized impurity donor scattering in the AlGaAs at the hetero-interface. The doped AlGaAs layer is around 500 \( \AA \) thick. This is followed by a heavily doped \( n^+ \) cap layer. The purpose of the cap layer is to facilitate ohmic contacts to source and drain. The gate materials include Ti, Mo, WSi, W or Al. The source and drain implantation is made after the gate is defined. Since high temperature anneal is needed to activate the dopants, refractory gate material is required. A cross sectional view of a typical HFET was shown in Figure 1.1. The energy band diagram for this structure is shown in Figure 2.1. Electrons from the ionized donor in the wide gap semiconductor (\( n'^{+} \)-AlGaAs) accumulate in the conduction band states of the narrow gap semiconductor (GaAs) because of the requirement of Fermi energy level to be constant throughout the structure. Since the electrons are confined to the potential well in the direction from the gate to the substrate (x direction), the electrons are free to move only in the width (y) and channel length (z) directions. Hence, these electrons are called 2-D electrons or 2-D electron gas (2DEG). Since the 2DEG is formed in the undoped GaAs layer, far away from the ionized donor impurities in the AlGaAs, the electrons travel with essentially no scattering due to ionized impurities. Furthermore, since an undoped AlGaAs spacer layer separates the \( n'^{+} \)-AlGaAs layer from the the 2DEG, the scattering is minimized at the hetero-interface, and the electron mobility and hence the transconductance is enhanced significantly. As in a MOSFET, the density
Figure 2.1: A schematic diagram illustrating the energy band diagram of a conventional HFET

n+AlGaAs  UNDOPED AlGaAs  UNDOPED GaAs  SUBSTRATE

2DEG  E_F  E_{g2}

E_{g1}

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of electrons in the channel and therefore the current can be modulated by application of a voltage to the gate.

2.4 Family of HFET devices

A few variants of the basic HFET structure are the single quantum well HFET, $I^2$-HEMT, doped channel HFET, heterostructure insulated-gate field effect transistor (HIGFET) and semiconductor-insulator-semiconductor field effect transistor (SISFET). These devices are described briefly below.

In a single quantum well HFET, the GaAs conducting channel is bounded on each side by AlGaAs layers. The AlGaAs layers are doped to maximize the carrier concentration in the channel layer. The sheet concentration is twice that of the conventional device [32]. The characteristic feature of this device are higher effective carrier velocity due to electron screening.

In a $I^2$-HEMT, the conducting channel is placed between an undoped AlGaAs layer and an $n^+$-AlGaAs layer. The gate is placed on the undoped AlGaAs layer. The $I^2$-HEMT has a small gate leakage under forward bias.

In a doped channel HFET [33, 34, 35, 36, 37], the channel (GaAs) is heavily doped and the gate is deposited on an undoped AlGaAs layer which acts as an insulator. The doped channel scheme reduces the electron mobility in the channel. But excellent high power operation shows that the total sheet charge density and the carrier confinement are more important than electron mobility. The gate-drain breakdown voltage is superior to that of a conventional HFET because the gate contact is on undoped AlGaAs.

A HIGFET differs from the basic HFET structure in that the GaAs and AlGaAs layers are undoped. The advantage of HIGFET is better control of the threshold voltage for complementary circuits in which n-channel and p-channel devices are
fabricated simultaneously.

A SISFET is similar to HIGFET except that the gate material contacting the undoped AlGaAs layer is another semiconductor that is usually the same as the channel layer, and is heavily doped.

### 2.5 HFET based on AlInAs/GaInAs material system

One way of improving the performance of HFETs is to use GaInAs as the 2DEG channel layer instead of GaAs. Benefits of a GaInAs channel include the enhanced electron transport in GaInAs as compared to GaAs and improved confinement of carriers in the quantum well, and larger conduction band discontinuity, \( \Delta E_c \), at the AlGaAs/GaInAs hetero-interface which allows higher sheet charge density and transconductance as compared to the AlGaAs/GaAs system. Typically a GaInAs layer is inserted between the AlGaAs and GaAs layers of a conventional HFET. Such an HFET is called a pseudomorphic HFET. Since the thin pseudomorphic GaInAs layer has a lattice mismatch with the surrounding layers, the strain from the mismatch predominantly resides in GaInAs. There is an upper limit on the thickness of the GaInAs layer beyond which the strain is not elastically accommodated and relieved by creation of dislocation which are line defects and act as traps for carrier. This upper limit decreases with increasing InAs mole fraction as the lattice mismatch increases. Higher InAs mole fraction is desirable to improve the transport properties of the carrier. At the same time, the GaInAs layer should not be so thin as to reduce the carrier confinement in the well. AlInAs/GaInAs heterostructures lattice matched to InP substrate can be fabricated with a higher percentage of InAs in GaInAs than can be achieved by strained GaInAs layers grown on GaAs.

InP has a lattice constant close to an alloy composed of 53 \% InAs and 47 \% GaAs. AlInAs is used as the high bandgap material. \( \Delta E_c \) at the AlInAs/GaInAs
hetero-interface is about 0.5 eV, whereas, $\Delta E_c$ at the AlGaAs/GaAs hetero-interface is about 0.25 eV. The higher $\Delta E_c$ in case of AllnAs/GalnAs system allows for higher sheet carrier concentration. The higher sheet carrier concentration along with the higher 300 K mobility of electrons in GaInAs leads to a more than a factor of two higher conductivity in the channel as compared to the AlGaAs/GaAs system. Additionally, the peak velocity of electrons in GaInAs is higher than in GaAs. In short-gate devices where the average velocity under the gate is closer to the peak velocity, electron transit times in GaInAs will be significantly smaller. Devices fabricated from GaInAs/AllnAs modulation doped structures currently exhibit the highest current gain cut-off frequency ($f_T = 250$ GHz for 0.1 $\mu m$ gate) [38] and lowest noise figure (0.8 dB at 60 GHz) [1] of any device. Digital circuits also exhibit the fastest switching speeds (4 ps at 300 K) [39].

2.6 Models for leakage gate current

The gate current in a heterostructure FET has been modeled based on thermionic emission and quantum tunneling mechanisms [5, 14, 15, 16, 17, 21, 22]. These models have been shown to be good for certain heterostructures. The transmission coefficient, which is the probability of an electron tunneling through a barrier, is used for the tunneling current computation, in the quantum tunneling models. The transmission coefficient was calculated either using the WKB approximation or by solving the Schroedinger equation.

The WKB approximation is based upon the assumption that the potential varies very slowly over lengths compared to the wavelength of the electron. The transmission coefficient is given by the WKB approximation as [42]:

$$T(E) \approx \exp \left[ -2 \int_{x_1}^{x_2} |\alpha(x)| dx \right],$$

where
where $U(x)$ is the gradually varying potential energy, $E$ is the energy of the electron, $m_n$ is the effective mass of the electron and $h$ is the Planck's constant. Kamada et al. [5] calculated the transmission coefficient in a HIGFET using the WKB approximation. The assumption of gradually varying potential may not be true at very high gate biases [18], where the potential drop in the various layers of the HFET can be quite sharp.

The other method for calculating the transmission coefficient is based on the solution of the Schroedinger equation. Chandra and Eastman [19] calculated the transmission coefficient for a triangular barrier by solving the Schroedinger equation using a numerical method. Gundlach [20] used the Airy function to yield the exact solution of the Schroedinger equation for a trapezoidal barrier. The solution to the Schroedinger equation can be obtained in terms of the Airy function for only linear potential profiles. However, the solution using Airy function is unsuitable for nonlinear structures like superlattice structure.

One of the first gate current models for HIGFETs was proposed by Baek et. al. [21]. In this model, the mechanisms of current were described by equations for high and low temperatures and for voltages above and below threshold. An improvement on this model was proposed by the same group [22]. In this model the 2-D electron density in the potential well was approximated using the 2 lowest subbands. The gate current was modeled as a diode equation with appropriate ideality factor. The model was more accurate and easier to manipulate than the previous model but it failed to describe the current in the subthreshold region. In 1990, Ruden [23] proposed a model based on the gradual channel approximation. Ruden modeled the gate current using a diode equation with 4 fitting parameters. Though the model
describes the gate current above and below threshold, it only gives a semiempirical estimate of the gate leakage current. In 1991, Fawaz et al. [16] introduced a quantum 2-D model based on the numerical solution of Schroedinger and Poisson equations. Soon after, Abbot et al. [17] proposed a quantum gate current model based on charge control analysis and the WKB approximation. The last two models did not consider the subthreshold region at all. Martinez et al. [24] proposed a model based on the self-consistent approximation of Schroedinger and Poisson equations. Four parameters were used to fit the model. Most of the models above make use of fitting parameters to model the gate current. The model developed in this thesis does not make use of any fitting parameters. The calculation of gate current takes into account both the quantum mechanical tunneling current and the thermionic emission current. The tunneling current is calculated using self-consistent solution to Schroedinger and Poisson equations.
CHAPTER 3

LEAKAGE GATE CURRENT CALCULATION

3.1 Introduction

In this chapter the various physical components of the leakage gate current, i.e. 2-D tunneling, 3-D tunneling and thermionic emission currents, are described and an analytical expression for leakage current due to each of the components is derived in terms of the device parameters and applied gate voltage. Some of these calculations require the conduction band edge profile and the allowed energies and the corresponding wave function. The procedure to obtain the conduction band edge profile of the HIGFET by a self-consistent solution to Poisson and Schroedinger equations along with the numerical procedure is described. Additionally, the numerical procedure for obtaining the total gate current, $I_g$ versus $V_g$ is also presented.

3.2 Self Consistent Solution to the Poisson and Schroedinger Equations

In order to get an analytical expression for various components of leakage gate current, the spatial and energy distributions of electrons within the device should be known. This requires the solution to the Schroedinger equation which provides the spatial electronic wave function for calculating the spatial 2-D electron density. The solution to the Schroedinger equation, in turn, requires the knowledge of conduction band edge profile. However, the determination of conduction band profile requires the solution to the Poisson equation, which, in turn, requires knowledge of the spatial distribution of electrons. This interdependent relationship between the Schroedinger
and Poisson equations can be visualized as shown in Figure 3.1. In Figure 3.1, \( E_c(x) \) is

\[
\begin{align*}
\text{Poisson's equation} & \quad \text{Output: } E_c(x) \\
\text{Input: } n_{2D}(x) & \\
\text{Schroedinger's equation} & \quad \text{Inputs: } n_{2D}(x), N_{2D,i}, \psi(E_i, x) \\
\text{Input: } E_c(x) &
\end{align*}
\]

Figure 3.1: A schematic diagram illustrating the interdependence of Schroedinger and Poisson equations.

the conduction band profile, \( n_{2D}(x) \) is the spatial 2-D electron density, \( E_i \) is the eigen energy satisfying the Schroedinger equation, \( \psi(E_i, x) \) is the wavefunction corresponding to \( E_i \) and \( N_{2D,i} \) is the sheet electron concentration corresponding to \( E_i \). In other words, the correct solution should satisfy both the Poisson and Schroedinger equations simultaneously. Thus, a self-consistent solution to the Poisson and Schroedinger equations is required. The numerical procedure for obtaining such a self-consistent solution is described in sections 3.3-3.6.

3.3 Solution to the Schroedinger Equation

The numerical technique used for the solution of the Schroedinger equation is based on a method by Ghatak et al. [41]. The method involves straightforward multiplication of \( 2 \times 2 \) scatter matrices, which describe the potential structure at a given point, without any iterations. The wave-function associated with an electron of energy \( E \), subjected to a potential \( E_c(x) \), obeys the time-independent Schroedinger
equation given by:

\[
\frac{\hbar^2}{2m_n} \frac{d^2 \psi(x)}{dx^2} + [E - E_c(x)] \psi(x) = 0
\]

(3.1)

where \( \hbar \equiv \frac{\hbar}{2\pi} \), \( \hbar \) being the Planck's constant, \( m_n \) is the effective mass of the electron and \( \psi(x) \) is the wave function. The conduction band edge profile, \( E_c(x) \), in a metal-insulator-semiconductor heterostructure is schematically represented in Figure 3.2.

![Figure 3.2: A schematic representation of the conduction band edge profile for a heterostructure device.](image)

In order to obtain a numerical solution of the Schrödinger equation for this potential structure, the problem is spatially discretized by considering piecewise constant potential profiles as shown in Figure 3.3. Within each discretized spatial region, the solution to the Schrödinger equation 3.1 is given by:

\[
u_j = \nu_j^+ e^{ik_j(x-\Delta_j)} + \nu_j^- e^{-ik_j(x-\Delta_j)},
\]

(3.2)

where
Figure 3.3: A schematic of diagram of the spatial discretization of the potential profile corresponding to a heterostructure.
\[ k_j = \left[ \frac{2m}{\hbar^2} (E - E_{c,j}) \right]^{\frac{1}{2}} \]

and

\[ \Delta_j = (j - 1)d, \quad j = 1, 2, \ldots, N \]

with \( u_j^+ \) and \( u_j^- \) representing the amplitudes of the waves propagating along the +x and -x directions, respectively. Continuity of \( u \) and \( du/dx \) at each interface results in [41]:

\[
\begin{pmatrix}
  u_1^+ \\
  u_1^-
\end{pmatrix} = S_1 \begin{pmatrix}
  u_2^+ \\
  u_2^-
\end{pmatrix} = S_1 S_2 \begin{pmatrix}
  u_3^+ \\
  u_3^-
\end{pmatrix} = \cdots = S_1 S_2 \cdots S_{N-1} \begin{pmatrix}
  u_N^+ \\
  u_N^-
\end{pmatrix},
\]

(3.3)

where

\[ S_j = \frac{1}{t_j} \begin{pmatrix}
  e^{-i\delta_j} & \gamma_j e^{-i\delta_j} \\
  \gamma_j e^{i\delta_j} & e^{i\delta_j}
\end{pmatrix} \]

and

\[ \delta_j = k_j d, \quad \gamma_j = \frac{k_j - k_{j+1}}{k_j + k_{j+1}} \quad \text{and} \quad t_j = \frac{2k_j}{k_j + k_{j+1}} \]

\( j = 1, 2, \ldots, N - 1, \quad N \) being the total number of regions. In the last region \( N \), the \( u_N^- \) term should vanish. Using this condition, the amplitudes, \( u_j^+ \) and \( u_j^- \), of the wavefunction in any region, \( j \), can be found in terms of \( u_1^+ \).

### 3.4 Spatial 2-D Electron Density

The spatial 2-D electron density, based on the 2-D density of states and Fermi-Dirac statistics, can be calculated as [42]:

\[ n_{2D}(x) = \sum_i \frac{m_i}{\pi \hbar^2} kT \ln \left( 1 + \exp \left( \frac{E_F - E_i}{kT} \right) \right) |\psi_i(x)|^2, \quad (3.4) \]
where \( k \) is the Boltzmann constant, \( T \) is the temperature in Kelvin, \( E_F \) is the Fermi energy which is characteristic of the material and its doping level, \( E_i's \) are the eigen energies and \( \psi_i(x) \) are the corresponding normalized wavefunctions obtained as solution to the Schroedinger equation 3.1.

3.5 Solution to the Poisson Equation

The solution to the Poisson equation is based on the following iterative numerical method for solving 2\(^{nd}\) order differential equation with 2 boundary conditions. The electric field, \( \varepsilon_s(x) \), in a semiconductor is given by the Poisson equation as:

\[
\frac{d\varepsilon_s(x)}{dx} = \frac{\rho(x)}{\varepsilon},
\]

where

\[
\rho(x) = \rho_{2D}(x) + \rho_{3D}(x) + qN_d
\]

with the charge due to positive ionized donors = \( qN_d \), the 2-D charge density, \( \rho_{2D}(x) = -qn_{2D}(x) \) and the 3-D charge density, \( \rho_{3D}(x) \), given by [43]:

\[
\rho_{3D}(x) = -qN_c\mathcal{F}_{\frac{1}{2}}\left(\frac{E_F - E_c(x)}{kT}\right)
\]

\[
= -qN_c\mathcal{F}_{\frac{1}{2}}\left(\frac{-R(x)}{kT}\right)
\]

with

\[
R(x) = E_c(x) - E_F
\]

and

\[
N_c = 2 \left(\frac{m_0kT}{2\pi\hbar^2}\right)^{\frac{3}{2}}
\]

\( \mathcal{F}_{\frac{1}{2}} \) in equation 3.7 is the \( \frac{1}{2} \) order Fermi integral details of which can be found in Ref [44]. The electric field intensity normal to the insulator-semiconductor interface,
\( \varepsilon_s(x) \), is given by:

\[
\varepsilon_s(x) = -\frac{dV(x)}{dx} = \frac{1}{q} \frac{dE_s(x)}{dx} = \frac{1}{q} \frac{d}{dx} [E_s(x) - E_F] \quad \text{(as } E_F \text{ is constant with } x)
\]

\[
= \frac{dR(x)}{dx}
\]

(3.8)

Combining equations 3.5 and 3.8 results in:

\[
\frac{d^2 R(x)}{dx^2} = \frac{\rho(x)}{\varepsilon_s}
\]

(3.9)

The solution to the Poisson equation 3.5 is obtained by solving equation 3.9 with the following boundary conditions at \( x=\infty \) (semiconductor bulk) and \( x=0 \) (semiconductor-insulator interface):

\[
R(\infty) = kT \ln \left( \frac{N_e}{N_d} \right)
\]

\[
\varepsilon_s(0) = \frac{\varepsilon_i(0) \epsilon_i}{\epsilon_s}
\]

(3.10)

where \( \varepsilon_s(0) \) and \( \varepsilon_i(0) \) are the electric fields in the semiconductor and insulator respectively at the insulator-semiconductor interface. The second boundary condition is a result of the equality of normal electric displacement vector at the insulator-semiconductor interface. To solve equation 3.9 numerically, the variables are discretized along the \( x \) axis and equations 3.5 and 3.8 are written, within each interval \( j \), as difference equations:

\[
\varepsilon_s(j - 1) = \varepsilon_s(j) - \frac{\Delta_{\text{step}} \rho(j)}{\epsilon_s}
\]

(3.11)

\[
R(j - 1) = R(j) - \Delta_{\text{step}} \varepsilon_s(j)
\]

(3.12)

where \( \Delta_{\text{step}} \) is the discretization interval.

The procedure for the numerical solution is as follows:
1. Apply the boundary condition at semiconductor bulk to obtain \( R(N - 1) \):
\[
R(N - 1) = kT \ln \left( \frac{N_e}{N_d} \right) \text{ and } \varepsilon_s(N - 1) \approx 0, \text{ where } N \text{ is the total number of intervals.}
\]

2. Start with \( R(N - 1) \) and \( \varepsilon_s(N - 1) \) to obtain \( R(j) \) and \( \varepsilon(j) \) within each interval, \( j \), using equations 3.11 and 3.12.

3. Check to see if \( \varepsilon_s(0) \) satisfies the boundary condition, \( \varepsilon_s(0) = \frac{\varepsilon_s(0)N_e}{\varepsilon_s} \). If it does, terminate. If it does not, then vary the number of points of discretization, \( N \), maintaining the value of \( \Delta_{\text{step}} \) and repeat steps 1 and 2.

A flow chart for the above procedure is shown in Figure 3.4.

3.6 Numerical technique for self-consistent solution to the Schroedinger and Poisson equations

As discussed in section 3.2 the conduction band edge profile must satisfy both the Poisson and Schroedinger equations requiring a self-consistent solution. The numerical technique for solving the Poisson and Schroedinger equations self-consistently is summarized below.

1. Start with \( \rho_{2D}(x) = 0 \) and solve the Poisson equation to obtain the conduction band edge profile.

2. Using the conduction band edge profile obtained from solution of the Poisson equation, solve the Schroedinger equation to get the 2-D charge density \( (\rho_{2D}(x)) \).

3. Add \( \rho_{2D}(x) \), \( \rho_{3D}(x) \) and \( qN_d \) to obtain \( \rho(x) \). Solve the Poisson equation. If the conduction band edge profile obtained from the solution of the Poisson equation is the same as the one obtained in the previous iteration, terminate. If not, go to step 2.
Figure 3.4: A flowchart illustrating the procedure for numerical solution of the Poisson equation.
A flow chart for the above procedure, for a self-consistent solution, is shown in Figure 3.5.

3.7 Leakage Gate Current

Referring to Figure 3.6, the gate current in HIGFET has 3 important components with identifiable physics. The components are:

1. current due to electrons having sufficient thermal energy to overcome the potential barrier at the insulator-semiconductor interface (thermionic emission), $I_{\text{therm}}$,

2. current due to elastic tunneling of 3-D electrons with energies greater than $E_{c,\text{bulk}}$ but less than the potential barrier $E_{\text{max}}$ at the semiconductor-insulator interface, $I_{3D}$ and

3. current due to elastic tunneling of quasi-bound 2-D electrons, in the accumulation well, from semiconductor to metal, $I_{2D}$.

Thus,

$$I_g = I_{\text{therm}} + I_{3D} + I_{2D} \quad (3.13)$$

A detailed discussion of these components of the gate current is presented in sections 3.8-3.10.

3.8 Gate Current due to Thermionic Emission

The thermionic emission current density, shown pictorially in Figure 3.6, is given by [44]:

$$I_{\text{therm}} = \int_{v_{\text{min}}}^{\infty} qv_z n(v_z) dv_z, \quad (3.14)$$
Figure 3.5: A flowchart illustrating the numerical technique for the self-consistent solution of the Schroedinger and Poisson equations.

Eg(x,i) = (x,i-l) & i\neq0

Solve the Poisson eqn. with 
\rho(x) = \rho_{2D}(x) + \rho_{3D}(x) + qN_d
to obtain E_c(x,i)

E_c(x,i) = E_c(x,i-1) & i\neq0?

Solve the Schroedinger eqn.
to obtain \rho_{2D}(x);

i = i + 1
Figure 3.6: A pictorial representation of the thermionic emission, 2-D tunneling and 3-D tunneling current components of the leakage gate current.
where

\[ v_{\text{min}} = \sqrt{\frac{2E_{\text{bar}}}{m_n}}, E_{\text{bar}} = E_{\text{max}} - E_{c, \text{bulk}} \]

and

\[ n(v_z) = \left( \frac{kT m_n^2}{2\pi^2 \hbar^3} \right) e^{\frac{E_{F} - E_{c, \text{bulk}}}{kT}} e^{-\frac{m_n v_z^2}{2kT}} \]

Evaluating the integral, given by equation 3.14, \( I_{\text{therm}} \) is given by:

\[ I_{\text{therm}} = \frac{q(kT)^2 m_n}{2\pi^2 \hbar^3} e^{\frac{E_{F} - E_{c, \text{bulk}}}{kT}} e^{-\frac{E_{\text{bar}}}{kT}} \]  \[ (3.15) \]

3.9 Tunneling current due to 3-D electrons

The tunneling current density due to 3-D electrons with energy above \( E_{c, \text{bulk}} \) (Figure 3.6) is given by [45]:

\[ I_{3D} = \int_{E_{c, \text{bulk}}}^{E_{\text{max}}} N(E)T(E)dE \]  \[ (3.16) \]

where

\[ N(E) = \frac{m_n q}{2\pi^2 \hbar^3} \int_{0}^{\infty} [f(E) - f(E + qV_g + E_{c, \text{bulk}} - E_F)]dE \]

\[ = \frac{m_n qkT}{2\pi^2 \hbar^3} \ln \left( \frac{1 + \exp \left( \frac{E_{F} - E}{kT} \right)}{1 + \exp \left( \frac{E_{F} - qV_g - kT \ln \left( \frac{N_F}{N_d} \right)}{kT} \right)} \right) \]

with \( T(E) \) in equation 3.16 representing the transmission coefficient of the 3-D electrons tunneling from semiconductor to the metal. \( T(E) \) is given by:

\[ T(E) = \left| \frac{u_N^+}{u_1^+} \right|^2 \]  \[ (3.17) \]

where, \( u_N^+ \) and \( u_1^+ \) are the components of the wavefunction, defined by equation 3.2, along the +x direction in the \( N^{th} \) and 1\(^{st} \) regions respectively in figure (3.3). For the case of 3-D electrons \( E \) varies from \( E_{c, \text{bulk}} \) to \( E_{\text{max}} \), which are limits of the integration given by equation 3.16.
3.10 Tunneling current due to 2-D electrons

The tunneling current density due to 2-D electrons in the accumulation well (Figure 3.6) is given by [46]:

\[ I_{2D} = \sum_{i} \left( \frac{qN_{2D,i}}{\tau_{e,i}} \right) \]  

(3.18)

where \( N_{2D,i} \) is the sheet electron concentration corresponding to \( i^{th} \) resonant level and is given by:

\[ N_{2D,i} = \frac{m_e k T}{\pi \hbar^2} \ln \left( 1 + e^{\frac{E_i - E}{k T}} \right) \]  

(3.19)

with \( E_i \) the resonant levels of the wavefunction in the accumulation well. In equation 3.18, \( \tau_{e,i} \) is the escape time of electrons from the \( i^{th} \) resonant state and is given by[47]:

\[ \tau_{e,i} = \frac{\hbar}{\Delta E_i} \]  

(3.20)

\( \Delta E_i \) is the full width at half maximum (FWHM) of the resonant peaks obtained by plotting the transmission coefficient \( T(E) \) as a function of \( E \). As in the case of 3-D electrons, the transmission coefficient for 2-D electrons in the accumulation well is given as:

\[ T(E) = \left| \frac{u_N^+}{u_1^+} \right|^2 \]

where \( E \) varies from the bottom of the accumulation well to the top of the accumulation well. Plotting the transmission coefficient, \( T(E) \) versus \( E \), we obtain Lorentzians of the form [41]

\[ T(E) = \left| \frac{u_N^+}{u_1^+} \right|^2 = \frac{A}{\gamma^2 + (E - E_i')^2} \]  

(3.21)

where \( E = E_i' \) represents the position of the peak and \( \Delta E_i = 2\gamma \) is the full width at half maximum (FWHM). The parameters \( E_i' \), \( A \) and \( \gamma \) (\( \Delta E_i \)) are obtained by fitting Lorentzians given by equation 3.21 to peaks in the plot of \( T(E) \) versus \( E \).

Thus in order to obtain the 2-D current density the following procedure is adopted:

1. obtain the transmission coefficient \( T(E) = \left| \frac{u_N^+}{u_1^+} \right|^2 \) as a function of \( E \), where \( E \) varies from bottom of accumulation well to the top of the accumulation well.
2. fit Lorentzians of the form of equation 3.21 to the peaks in the plot of $T(E)$ and obtain $A$, $E'_s$ and $\Delta E_i$.

3. using equations 3.20, 3.19 and 3.18, calculate the 2-D current density $I_{2D}$. 

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CHAPTER 4

RESULTS, COMPARISONS AND DISCUSSIONS

4.1 HIGFET based on AlInAs/GaInAs material system

The first HIGFET structure considered in this work was based on AlInAs/GaInAs material system which was experimentally studied and reported in literature [5]. The material and geometrical parameters describing the device structure are listed in Table 4.1.

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Parameter symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>$T$</td>
<td>300 K</td>
</tr>
<tr>
<td>Conduction band discontinuity</td>
<td>$\Delta E_c$</td>
<td>0.52 eV</td>
</tr>
<tr>
<td>Schottky barrier height</td>
<td>$\phi_s$</td>
<td>0.57 eV</td>
</tr>
<tr>
<td>Thickness of the insulator</td>
<td>$d$</td>
<td>300 Å</td>
</tr>
<tr>
<td>Energy gap</td>
<td>$E_g$</td>
<td>0.75 eV</td>
</tr>
<tr>
<td>Effective mass of electron in GaInAs</td>
<td>$m_s$</td>
<td>0.041 $m_o$</td>
</tr>
<tr>
<td>Effective mass of electron in AlInAs</td>
<td>$m_i$</td>
<td>0.084 $m_o$</td>
</tr>
<tr>
<td>Donor concentration in GaInAs</td>
<td>$N_D$</td>
<td>$4.3 \times 10^{21}$ /m$^3$</td>
</tr>
<tr>
<td>Donor concentration in AlInAs</td>
<td>$N_D$</td>
<td>$1.0 \times 10^{21}$ /m$^3$</td>
</tr>
</tbody>
</table>

The applied gate voltage range of this study was 0.1-1.5 V. Equations 3.1 and 3.5 were solved self-consistently using the numerical technique described in section 3.6 to obtain the energy band profile, the 2-D energy states and spatial and energy distributions of electrons. Due to the failure of the non-degenerate statistics near the semiconductor-insulator interface, a Fermi integral table was created for the energy...
range -20 kT to 20 kT, to be used as a look-up table for the numerical solution.

The value of \((E_c - E_F)\) in the GaInAs bulk is same for all the gate voltages. This is consistent with the fact that the conduction band edge profile has to satisfy the boundary condition in the bulk dictated by equation 3.10. It is noted that the surface band bending for larger \(V_g\) is larger as expected. Also, for most \(V_g\)s, the width of the accumulation layer is about 500 Å. In other words, the distance between the quasi-neutral bulk to the semiconductor-insulator interface is 500 Å which is also the width of the accumulation well. The profile of \(E_c(x)\) versus \(x\), obtained from the self-consistent solution, is shown in Figure 4.1 for applied gate voltages, \(V_g = 0.4\) V and \(V_g = 0.88\) V, respectively. All the above observations are seen in Figure 4.1. The surface band bending is 0.19 eV and 0.27 eV for \(V_g = 0.4\) V and \(V_g = 0.88\) V, respectively. Also, as seen in the figure, the conduction band edge goes close to its bulk value within a relatively short distance from the semiconductor-insulator interface. This region is the accumulation well and its width increases slightly with increasing \(V_g\) as seen in the figure.

The electric field intensity, \(\varepsilon_s(x)\), goes to zero in the semiconductor bulk and satisfies the boundary condition, given by equation 3.10, at the semiconductor-insulator interface. The electric fields are largest at the GaInAs-AlInAs interface as expected. The peak electric field ranges from \(3.33 \times 10^6\) to \(4.33 \times 10^7\) V/m for the range of applied gate voltages. The profile of \(\varepsilon_s(x)\) versus \(x\), obtained from the self-consistent solution, is shown in Figure 4.2 for applied gate voltages, \(V_g = 0.4\) V and \(V_g = 0.88\) V, respectively. The above observations are seen in Figure 4.2. The peak electric fields are \(9.99 \times 10^6\) and \(2.33 \times 10^7\) V/m for gate voltages, \(V_g = 0.4\) V and \(V_g = 0.88\) V, respectively. As in the case of \(E_c\), the electric field intensity also goes rapidly to the bulk value within the accumulation well width.

The wavefunction, which provides information about the spatial and energy dis-
Figure 4.1: The conduction band edge profile obtained from a self-consistent solution of Poisson and Schroedinger equations for $V_g = 0.4$ V and $V_g = 0.88$ V. The Fermi level $E_F$ is assumed to be the reference zero for energy. $x=0$ corresponds to the AlInAs-GaInAs interface and positive $x$ is in the semiconductor GaInAs.
Figure 4.2: The electric field intensity profile obtained from a self-consistent solution to Poisson and Schroedinger equations for $V_g = 0.4 \text{ V}$ and $V_g = 0.88 \text{ V}$. $x=0$ corresponds to the AlInAs-GaInAs interface and positive $x$ is in the semiconductor GaInAs.
tribution of 2-D electrons, is obtained by solving the Schroedinger equation. It is noted that, for a given $V_g$, the number of nodes in the wavefunction solution increases with increasing eigen energies. This happens because the width of the accumulation well increases with increasing eigen energies. The wavefunction decays rapidly to zero outside the accumulation well indicating that an electron at that eigen energy level has very small probability of existing outside the accumulation well. This explains the accumulation of electrons in the accumulation well. The wave function, $|\Psi(x)|^2$, corresponding to $3^{rd}$ eigen energy, for applied gate voltages, $V_g = 0.4$ V and $V_g = 0.88$ V, are shown in Figures 4.3 and 4.4 respectively. The above observations are seen in the figure. As seen in the figure, the wavefunctions for both the $V_g$s have three nodes. It is also seen from the figure that, within the accumulation well, the magnitude of the wavefunction reduces, away from the bulk and towards the semiconductor-insulator interface.

The 2-D electron concentration profile, obtained from equation 3.4, peaks inside the accumulation well as expected from the wavefunction solution. The peak 2-D electron concentration increases with increasing gate voltage. The distribution of 2-D electrons, shown in Figures 4.5 and 4.6, demonstrates the accumulation of electrons, in the potential well, close to the semiconductor-insulator interface. The above observations are seen in the figure. The peak value of 2-D electron concentration is $1.59 \times 10^{23}$ /m$^3$ for $V_g = 0.4$ V and $5.42 \times 10^{23}$ /m$^3$ for $V_g = 0.88$ V. As seen in the figure, the peak of the 2-D concentration profile occurs very close to the semiconductor-insulator interface. From this observation and the plot of the wavefunction inside the accumulation well it can be inferred that the lowest eigen states contribute the maximum 2-D electrons. This, in-fact, is true and is confirmed by equation 3.4.

The sheet carrier concentration, $n_s$, is obtained by integrating the 2-D electron concentration from semiconductor-insulator interface to semiconductor bulk. $n_s$ in-
Figure 4.3: The wave function corresponding to 3rd eigen energy for an applied gate voltage of 0.4 V.
Figure 4.4: The wave function corresponding to 3rd eigen energy for an applied gate voltage of 0.88 V.

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Figure 4.5: The 2-D electron distribution for an applied gate voltage of 0.4 V.
Figure 4.6: The 2-D electron distribution for an applied gate voltage of 0.88 V.
creases almost linearly with the applied gate voltage. This is expected since a higher positive voltage on the gate capacitively induces more negative charge in the accumulation well to maintain charge neutrality throughout the system. $n_s$ is plotted as a function of $V_g$ in Figure 4.7. The calculated values were computed at 300 K and open drain conditions. The calculated value of $n_s$ is about $5 \times 10^{15}$ /m² at a gate voltage of 1 V. Figure 4.7 also shows the experimentally measured values of sheet carrier concentration as a function of the gate voltage [5]. The experimental values were obtained from Shubnikov-de-Haas oscillations measured at 3.2 K, with a drain voltage of 0.02 V under magnetic fields up to 6.15 T. The experimental values at $T=300$ K and open drain conditions are not available for comparison.

![Figure 4.7: The relation between sheet carrier concentration and gate voltage.](image)

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The transmission coefficient, $T(E)$, is computed using equation 3.17. $T(E)$ exhibits peaks at the eigen energies. It is noted that the number of eigen energies increases with the applied $V_g$. This is expected as the accumulation well becomes deeper with increasing $V_g$. Since the number of eigen energies increases with increasing $V_g$, the number of peaks in the plot of $T(E)$ increases with increasing $V_g$. Also, the spacing between peaks decreases with increasing $E_i$. This is consistent with the solution of the Schroedinger equation in a finite potential well. $T(E)$ is plotted as a function of $E$ in Figures 4.8 and 4.9 for gate voltages $V_g = 0.4$ V and $V_g = 0.88$ V respectively. The above observations are seen in the figure. $T(E)$ corresponding to $V_g = 0.4$ V and $V_g = 0.88$ V exhibits 11 and 12 peaks respectively.

![Graph showing transmission coefficient as a function of energy for $V_g = 0.4$ V](image_url)

**Figure 4.8:** The transmission coefficient associated with electrons at various energy levels for $V_g = 0.4$ V. The transmission coefficient exhibits peaks at the resonant energy levels.
Figure 4.9: The transmission coefficient associated with electrons at various energy levels for $V_g = 0.88$ V. The transmission coefficient exhibits peaks at the resonant energy levels.
The peaks in the plot of $T(E)$ correspond to the eigen energies and are in the form of Lorentzians given by equation 3.21. The fitting of the peaks to Lorentzians was done using a numerical method based on least square error. The difference between the fitting Lorentzian and the corresponding points on the peak were squared and summed. This was done for points close to the tail of the peaks and the Lorentzian resulting in the minimum sum was taken as the best fit. Figure 4.10 shows a single peak corresponding to $E_i = 0.46675$ eV and $V_g = 0.4$ V fitted to a Lorentzian. The full

![Graph](image)

Figure 4.10: A single peak corresponding to an applied gate voltage of 0.4 V and $E_i = 0.46675$ eV fitted to a Lorentzian.

width half maximum (FWHM) width, $\Delta E_i$, for this peak, defined as $2\gamma$ in equation 3.21, was computed to be $4.22 \times 10^{-11}$ eV. The escape time of the electron from this resonant level, $\tau_{e,i}$, was computed to be $1.56 \times 10^{-5}$ sec. using equation 3.20. The sheet electron concentration, $N_{2D,i}$ was computed to be $5.3 \times 10^{13}$ /m$^2$ (equation 3.19).
The contribution to 2-D tunneling current due to this resonant state was computed (using one of the terms in the summation in equation 3.18) to be 0.546 A/m². The above fitting procedure and calculations were performed for all the peaks in the plot of $T(E)$ for each $V_g$. For a given $V_g$, it is noted that the peaks corresponding to eigen energies close to the top of the accumulation well contribute the most to the 2-D tunneling current.

Figure 4.11 shows the comparison of the thermionic emission (equation 3.15), 3-D tunneling (equation 3.16) and 2-D tunneling (equation 3.18) currents as a function of $V_g$. The curve for the 2-D tunneling current has an estimated margin of error of ±1 order of magnitude. The error arises from the difficulty in fitting the peaks in the plot of $T(E)$ versus $E$ to Lorentzians in order to calculate the escape time of the electrons from the resonant states. For all the gate voltages considered, few of the peaks, corresponding to eigen energies at the top of the accumulation well, did not fit well to Lorentzians using the criteria discussed earlier. As already noted these are the peaks that contribute the most to the 2-D tunneling current. Thus the calculated values could be off by ±1 order of magnitude. From Figure 4.11 it is clear that the 2-D tunneling current is the dominant component of the leakage gate current.

Figure 4.12 shows the total calculated current density due to all three components as a function of $V_g$. For reasons discussed above there is a margin of error of ±1 order of magnitude in the calculated leakage current. Figure 4.12 also shows the experimentally measured current density as a function of the gate voltage. The curve shows good agreement with the experimental curve. Even though there is an estimated error of ±1 order, the results obtained here are more accurate than the closest calculated values in previous literature, where the calculated currents are more than two orders off.
Figure 4.11: The 2-D tunneling, 3-D tunneling and thermionic emission current densities as a function of the gate voltage.
Figure 4.12: The total current density as a function of the gate voltage.
4.2 HIGFET based on AlGaAs/GaAs material system.

The second HIGFET structure considered in this work was based on AlGaAs/GaAs material system which was experimentally studied and reported in literature [21]. The material and geometrical parameters describing the device structure are listed in Table 4.2.

Table 4.2: Parameters for the AlGaAs/GaAs heterostructure system obtained from [21] and used for various calculations

<table>
<thead>
<tr>
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</tr>
</thead>
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<td>0.33 eV</td>
</tr>
<tr>
<td>Schottky barrier height</td>
<td>$q\phi_s$</td>
<td>1.2 eV</td>
</tr>
<tr>
<td>Thickness of the insulator</td>
<td>$d$</td>
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</tr>
<tr>
<td>Energy gap</td>
<td>$E_g$</td>
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</tr>
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<td>Effective mass of electron in GaAs</td>
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<td>0.067 $m_o$</td>
</tr>
<tr>
<td>Effective mass of electron in AlGaAs</td>
<td>$m_i$</td>
<td>0.092 $m_o$</td>
</tr>
<tr>
<td>Donor concentration in GaAs</td>
<td>$N_D$</td>
<td>Intrinsic</td>
</tr>
<tr>
<td>Donor concentration in AlGaAs</td>
<td>$N_D$</td>
<td>Intrinsic</td>
</tr>
</tbody>
</table>

Even though the GaAs layer was reported to be intrinsic, for the purpose of calculations, the GaAs layer was assumed to be doped n-type with a doping concentration of $1.0 \times 10^{21} /m^3$. This is reasonable, since, even the growth of an intrinsic crystal will result in some unintentional doping level in GaAs. The procedure for obtaining the 2-D tunneling, 3-D tunneling and thermionic emission currents was the same as for the AlInAs/GaInAs system.

The applied gate voltage range of this study was 0.9-1.4 V. The reason for the high value of the lower limit of $V_g$ for the AlGaAs/GaAs system is the large Schottky barrier height which limits the range of $V_g$ where the device operates as a HIGFET. The profiles discussed in Figures 4.1-4.12 are similar for the AlGaAs/GaAs system as for the AlInAs/GaInAs system. Additionally, most of the observations made in
profiles of Figures 4.1-4.12 for the AlInAs/GaInAs system hold for those profiles for the AlGaAs/GaAs system as well. Only the profiles having distinguishing features are discussed here.

The surface band bending, in the case of AlGaAs/GaAs system, is noted to be lesser than that for the AlInAs/GaInAs system for comparable $V_g$s. As an example, the surface band bending, for the AlGaAs/GaAs system, is 0.09 eV for an applied $V_g$ of 0.92 V, whereas, for the AlInAs/GaInAs system, it is 0.27 eV for an applied $V_g$ of 0.88V. The total number of eigen energies ranges from 9-12 for the AlInAs/GaInAs system, whereas, it ranges from 11-13 for the AlGaAs/GaAs system for the respective applied range of $V_g$s.

$n_s$ is plotted as a function of $V_g$ in Figure 4.13. Figure 4.13 also shows the experimentally measured values of sheet carrier concentration as a function of the gate voltage [22] for a related system. The calculated curve shows good linear behaviour, however, it deviates from the experimental curve for increasing $V_g$. This is attributed to the possible error in the assumption of the donor doping level in the GaAs semiconductor. Figure 4.14 compares $n_s$ for the AlGaAs/GaAs and AlInAs/GaInAs systems. As can be seen, $n_s$ for the AlInAs/GaInAs system is higher for comparable gate voltages.

Figure 4.15 shows the comparison of the thermionic emission (equation 3.15), 3-D tunneling (equation 3.16) and 2-D tunneling (equation 3.18) currents as a function of $V_g$. The curve for the 2-D tunneling current has an estimated margin of error of $\pm 1$ order of magnitude. The reason for the error again lies in the difficulty in fitting the peaks in the plot of $T(E)$ to Lorentzians.

Figure 4.16 shows the total calculated current density due to all three components as a function of $V_g$. There is a margin of error of $\pm 1$ order of magnitude in the calculated leakage current. Figure 4.16 also shows the experimentally measured current.
Figure 4.13: The relation between sheet carrier concentration and gate voltage.
Figure 4.14: Comparison of the sheet carrier concentration as a function of the gate voltage for the AlGaAs/GaAs and AlInAs/GaInAs systems.
density as a function of the gate voltage. The curve shows a similar pattern, however, it shows a large order of magnitude difference from experimental curve. This is attributed to an error in the assumed doping level in the GaAs semiconductor. The assumed doping level was higher than the doping level in the experimental structure. The calculations could not be performed for a lower doping level due to the following limitation.

The width of the accumulation well increases with decreasing doping concentration, $N_D$. For $N_D = 1.0 \times 10^{21} / m^3$, the width of the accumulation well is about 700 Å for most $V_g$s, whereas, for $N_D = 1.0 \times 10^{20} / m^3$, the width of the accumulation well is about 5000 Å for most $V_g$s. As was noted in Figures 4.3 and 4.4, the magnitude of the wavefunction increases away from the semiconductor-insulator interface and towards the bulk. For $N_D = 1.0 \times 10^{20} / m^3$, with an accumulation well width of about 5000 Å, the magnitude of the wavefunction becomes significantly large to exceed the numerical range of the computer, which is about $10^{300}$. Hence, calculations could not be performed with lower $N_D$s.
Figure 4.15: The 2-D tunneling, 3-D tunneling and thermionic emission current densities as a function of the gate voltage.
Figure 4.16: The total current density as a function of the gate voltage.
CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

The leakage gate current, $I_g$, versus the gate voltage, $V_g$, characteristics are studied for the AlInAs/GaInAs and AlGaAs/GaAs based HIGFETs assuming three important components of the leakage gate current, namely, 2-D tunneling, 3-D tunneling and thermionic emission current. The conduction band edge profile, the allowed energies and the corresponding wave functions are obtained by solving the Poisson and Schroedinger equations self-consistently. For the HIGFET based on the AlInAs/GaInAs material system, the agreement between the experiment and theory is excellent, and the currents are within a factor of 10 for most voltage ranges. This is more accurate than the results obtained in previous literature [5], where the currents are off by more than a factor of 100 for most voltage ranges. The reason for discrepancy between experiments and theory in [5] is mainly due to the exclusion of the 2-D tunneling current from the eigen states. For the HIGFET based on the AlGaAs/GaAs material system, the agreement between theory and experiment is poor. However, the behaviour of the wavefunction solution, the allowed energies, the sheet carrier concentration profile and current density profile were as expected. The reason for the disagreement of the above profiles from the experimental profiles is mainly attributed to an assumption of a higher doping concentration in the GaAs semiconductor. The exact doping concentration in the semiconductor for the AlGaAs/GaAs HIGFET system were not available.
5.2 Future Recommendations

The limitations of the numerical procedure, described in this work, for calculating the leakage gate current are enumerated below.

1. The calculation of the 2-D tunneling current, which is the dominant component of the leakage gate current, involves fitting Lorentzian to the peaks obtained in the transmission coefficient, $T(E)$, for calculating the escape time of the electrons from the resonant states. The fits were not good for some peaks and resulted in an anticipated error of $\pm 1$ order of magnitude in the calculated 2-D tunneling current.

2. For wide accumulation wells, the wavefunction amplifies significantly to exceed the numerical range of the computer. Thus, the procedure is limited to small accumulation widths.

Alternative methods of calculating the escape time of the electrons from the resonant states may be expected to provide more accurate results. Alternative numerical procedures for solving the Schroedinger equation can avoid the problem of exceeding the numerical range of the computer for structures having a large accumulation width. Finally, in the present work, the time-independent Schroedinger equation is solved and the information about time evolution of the electron position is incorporated through the escape time of the electron from the resonant states, which is an approximation. More accurate results can be obtained by solving the time-dependent Schroedinger equation and complex eigen energy approaches.
BIBLIOGRAPHY


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[40] F. Ali, A. Gupta, HEMTs and HBTs, Devices, Fabrication, and Circuits, Norwood, MA, Artech House, 1991


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