12-1-2016

An EMG-based patient monitoring system using Zynq SoC device

Farhad Fallahlalehzari
University of Nevada, Las Vegas

EMG-BASED PATIENT MONITORING SYSTEM USING ZYNQ SoC DEVICE

By

Farhad Fallahlalehzari

Bachelor of Electrical and Electronics Engineering
Islamic Azad University, Karaj branch, Iran
2013

A thesis submitted in partial fulfillment
of the requirements for the

Master of Science in Engineering- Electrical Engineering

Department of Electrical and Computer Engineering
Howard R. Hughes College of Engineering
The Graduate College

University of Nevada, Las Vegas
December 2016

UNLV | GRADUATE COLLEGE

Thesis Approval

The Graduate College
The University of Nevada, Las Vegas

December 1, 2016

This thesis prepared by

Farhad Fallahlalehzari

entitled

EMG-based patient monitoring system using Zynq SoC device

is approved in partial fulfillment of the requirements for the degree of

Master of Science in Engineering- Electrical Engineering
Department of Electrical and Computer Engineering

Sarah Harris, Ph.D.
Examination Committee Chair

Kathryn Hausbeck Korgan, Ph.D.
Graduate College Interim Dean

Shahram Latifi, Ph.D.
Examination Committee Member

Venkatesan Muthukumar, Ph.D.
Examination Committee Member

Stephen Benning, Ph.D.
Graduate College Faculty Representative

Abstract

This thesis describes the design, development, and testing of an EMG-based patient monitoring system using the Zynq device. Zynq is a system on chip device designed by Xilinx which consists of an ARM dual cortex-A9 processor as well as an FPGA integrated into one chip. This work also analyzes the performance of image-processing algorithms on this system and compares that performance to more traditional PC-based systems. Image processing algorithms, such as Sobel edge detection, dilation and erosion, could be used in conjunction with a camera for the patient monitoring purposes. These algorithms often perform sub-optimally on processors because of their high computation demand, thus they are excellent candidates for the hardware acceleration available on an FPGA. This analysis shows that the performance of these algorithms in hardware using the Zynq-based architecture perform about 1800 times faster than the MATLAB implementation and 40 times faster than the OpenCV implementation on the PC. Moreover, the power consumption of the Zynq device proved to be about six and five times less than PC-based implementation using MATLAB and OpenCV respectively. Thus, the Zynq-based patient monitoring system proved to be both higher performance and lower power than a processor-based system. Both factors, performance and power consumption, are crucial for patient monitoring because of the demand for mobility and battery-based systems.

Acknowledgements

Foremost, I would like to express my sincere gratitude to my advisor Dr. Sarah Harris for providing me with the guidance, motivation, and supervision to complete my research work. I could not have imagined having a better advisor for not only my research work, but also for learning morality and humanity for my entire life.

I am also so grateful to my thesis committee members Dr. Shahram Latifi for his guidance during my master's degree, Dr. Venkatesan Muthukumar for being supportive and helpful during my master's study, and Dr. Stephen Benning for involving me to his research lab and help me to get more familiar with the psychology instrumentation aspect of my research project.

Last but not least, I would like to kiss my parent's hands who have been taking care of me even now from the heaven, and thank to my kind and lovely fiancee Ms. Sara Dehghani, my family members, especially my supportive and compassionate sister, Ms. Farnaz Fallahlalehzari, for their never-ending help and encouragement to complete this degree.

Farhad Fallahlalehzari

University of Nevada, Las Vegas
December 2016

Table of Contents

Abstract ..... **iii**

Acknowledgements ..... **iv**

Table of Contents ..... **v**

List of Tables ..... **vii**

List of Figures ..... **viii**

Chapter 1 Introduction **1**

Chapter 2 Background **4**

2.1 Patient monitoring 4

2.2 Biomedical signals 5

2.2.1 EMG 6

2.2.2 EEG 7

2.2.3 ECG 7

2.3 Hardware acceleration 8

2.4 Zynq SoC structure 10

2.4.1 Application Processing unit (APU) 11

2.4.2 Programmable logic (PL) unit structure 12

2.4.3 AXI interconnection 13

2.4.4 PS and PL communication port 16

2.4.5 Zynq design flow 16

2.5 Image processing 17

Chapter 3 Methodology **19**

3.1 EMG signal acquisition 21

3.1.1 Skin noise elimination 21

3.1.2 Electrode-noise reduction 21

3.1.3 Electrode placement and routing . . . 22
3.2 Signal conditioning system . . . 23
3.2.1 Pre-amplifier . . . 24
3.2.2 Low pass filter . . . 25
3.2.3 High pass filter . . . 26
3.2.4 Differential amplifier . . . 27
3.3 Processing setup . . . 27
3.3.1 TySOM-1-7Z030 evaluation board . . . 27
3.3.2 ARM dual cortex A9 processor . . . 28
3.3.3 Analog to digital conversion (ADC) module . . . 29
3.3.4 Direct Memory Access (DMA) module . . . 30
3.3.5 Timer module . . . 30
3.3.6 Sobel edge detection, dilation, and erosion modules . . . 31
3.4 Applications . . . 33
3.5 CPU-based implementation . . . 33
3.6 Power performance analysis . . . 33

Chapter 4 Results and Discussion . . . 36
4.1 Image processing algorithms using Zynq device . . . 36
4.2 Image processing algorithms using personal computer . . . 37
4.3 Comparison of the Zynq and PC-based system performances . . . 37
4.4 Power consumption analysis . . . 38

Chapter 5 Conclusion and Future Work . . . 39

Bibliography . . . 40

Curriculum Vitae . . . 43

List of Tables

4.1 Execution time of the Zynq-based implementation 37
4.2 MATLAB execution time 37
4.3 Zynq and OpenCV comparison 38
4.4 Power consumption comparison 38

List of Figures

1.1 Global patient monitoring system block diagram 2

2.1 Bicep EMG signal acquisition system 6
2.2 EEG-based patient monitoring 7
2.3 ECG-based patient monitoring 8
2.4 Microprocessor and hardware accelerator connection 9
2.5 Zynq internals 11
2.6 Structure of the application processing unit 12
2.7 Structure of the programmable logic unit 13
2.8 AXI4 interconnection categories 14
2.9 AXI interconnection IP 15
2.10 Processing system and programmable logic communication ports 16
2.11 Zynq design flow hierarchy 17

3.1 Zynq-based patient monitoring system block diagram 19
3.2 An overview of the developed system 20
3.3 EMG electrode 22
3.4 Correct electrode attachment 23
3.5 Applied wire for transferring electrode signals to EMG acquisition circuit 23
3.6 EMG signal acquisition circuit 24
3.7 Structure of an instrumentation amplifier 25
3.8 Second order active low-pass filter 25
3.9 Second order active low-pass filter 26
3.10 Second order active high-pass filter 26
3.11 Second order active high-pass filter 27
3.12 TySOM-1-7Z030 evaluation board 28
3.13 Flowchart view of the developed system 29
3.14 Interface between acquired EMG signals and XADC 30

3.15 Zynq block diagram 32
3.16 Complete project block design by Vivado 32
3.17 Watt's Up meter connection to the TySOM-1-Z7030 board 34
3.18 Kill a Watt meter connection to the TySOM-1-Z7030 board 35

Chapter 1

Introduction

Knowledge or money, which one is better?" This is an old question that everybody has been asked or at least has thought about during their lives. With the explosion of information in the 21st century, and the pressure of worklife balance, perhaps we could add "health" to that question, "knowledge, money or health, which one is better?" It goes without saying that without being healthy, achieving knowledge or money is difficult, at best. However, there are many people who disagree with this fact, and they are expressing this by their actions such as hours of work just to make more money. From the point of view of a patient diagnosed with an illness, the answer would be definitely health as they know the worth of health more than others.

Factors such as genetic disorders, work stress, and unhealthy diet can increase the probability of illness. In addition, as our population ages, the demand for health care in the elder population increases. Subsequently, with increasing numbers of patients, physicians and hospitals come increasing demands on. Additionally, increasing healthcare costs, make treatment and health screening, out of reach for many patients. Remote patient monitoring has been proposed to meet this increased demand. It has also become more popular as a means of simplifying the healthcare process. Remote patient monitoring can not only meet the increased demand, but also increase overall efficiency by, for example, reducing travel and waiting time and decreasing the spread of infections diseases in doctor's waiting rooms.

Any patient monitoring system consists of signal acquisition and a processing section. To record the vital data from the patient's body, the patient monitoring system might include unit for detection of blood glucose level, heart rate and temperature. In some advanced systems, electroencephalography (EEG), electrocardiography (ECG) and electromyography (EMG) are used to monitor brain, heart and muscle activities respectively. The patient monitoring system updates the physician about the patients health status. Fig. 1.1, shows block diagram of a typical patient monitoring system.

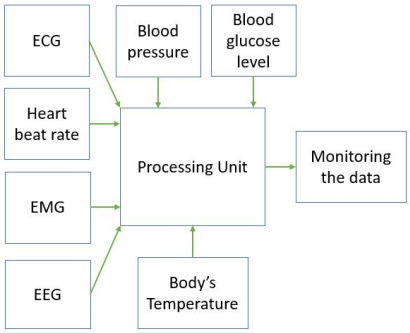

Figure 1.1: Global patient monitoring system block diagram

As shown in the above image, the acquired data from the patient's body is sent to a Processing Unit for analysis. By progression of the technology, these processing unit has also become high performance. Because the input data to these processing units are often wide, the more powerful the processing system is, the more reliable the patient monitoring system would be. In this regard, applying high performance processors to patient monitoring systems has become crucial.

This thesis proposes a patient monitoring system based on the Zynq SoC system. The unique aspect of combining a traditional processor with hardware acceleration for computational intensive algorithms on the on-board FPGA, offers a high performance, low power and low-cost solution compared to traditional PC-based patient monitoring systems.

With respect to the culture in which I was born and raised, Persian, caring was one of the major virtues that I was taught. A plethora of lessons exist from experienced people, including poems and stories in which sympathy was taught as one of the foundations of humanity. In this regard, I have always had this goal in my mind to make life easier for other human beings. As an electrical and computer engineering student, among various topics to pick, I aimed to choose a topic which would help the human race. In my case, having lived with a partially disable person, my brother, ignited the idea of making the world a more comfortable place for people with disabilities and others with health issues. My professional background of computer engineering along with my personal background choose and have given me strong motivation to pursue this master's topic related to patient monitoring system.

The main objective of this thesis is to design, develop and test a high-performance, low-power and low-cost EMG-based patient monitoring system in which some of the computationally algorithms are accelerated in hardware.

The reminder of this thesis is as follows; provides a background of patient monitoring systems and

hardware acceleration (Chapter 2),describes the developed patient monitoring system (Chapter 3), discusses the performance of the developed system (Chapter 4), and concludes (Chapter 5). A brief overview of each chapter is provided here.

Chapter 2 describes existing patient monitoring systems and the EMG, EEG and ECG biomedical signals that are used to monitor a patient. This chapter also studies the hardware acceleration and Zynq SoC device structure. Chapter 3 studies the patient monitoring system developed in this thesis. This chapter describes the hardware and software developed to receive EMG an video signals from the patient and process the signals. It also discusses the hardware versus software implementation of the Sobel edge detection, erosion, and dilation image-processing algorithms. This section concludes with a discussion of the power measurement instrumentation. Chapter 4 discusses and compares the performance and power consumption of the Zynq-based system to PC-based system. Chapter 5, summarizes the results of this thesis. It also discusses future steps and potential applications.

Chapter 2

Background

This chapter reviews the patient monitoring system and related works and biomedical signals including EMG, EEG and ECG. Additionally, we discuss hardware acceleration and the Zynq SoC system, the target hardware of the developed patient monitoring system. This chapter concludes with an overview of the three image-processing algorithms implemented in this thesis: Sobel edge detection, dilation, and erosion.

2.1 Patient monitoring

The decreased mobility of older patients combined with increased need for health monitoring suggests the need for remote patient monitoring which is called telemedicine. A patient monitoring system includes sensors to record the vita signals of a patient.

Home-healthcare in the shape of telemedicine is a tool to promote the importance of self-health monitoring which lead to earlier diagnosing of health problems. Significant reduction in the risk of health problems and the cost of transportation and time are considered the main benefits of remote patient monitoring systems [1]. Telemedicine offers not only health benefits to the patient but also lessens the carbon footprint by decreasing transportation needs, especially for non-emergency screening. Because of these advantages, patient monitoring systems have proliferated in the 21st century. A patient monitoring system that transfers images using Global System for Mobile (GSM), a system which transfers the biomedical signals including ECG and PC-based studied are discussed here.

A portable medical system that supports long distance consultation of expert physicians is developed in [2]. This system is able to transmit the vital biosignals of the patient along with the images of the patient's injured sites to a physician using Global System for Mobile (GSM) technology on mobile networks. Having used this system allows the emergency technicians to consult with the physicians while the patient is on the way to hospital. The performance of this system was evaluated in four countries on 100 patients in each

country. A system, in which shoulder replacement surgery patients are communicating asynchronously with their surgeons through a website, has been developed and tested in [3]. In this project, a web browser has made the process of capturing a video and send it to a web site simple for computer beginners. The designed web browser plug in is able to transfer any type of data from the patient to the website such as glucose level and spirometer. Both the patient and physician can access this website to monitor the patient's health status. This system has been tested on patients who both have no experience in working with computers and expert users. Results showed that all of the users were able to send at least one video massage to their physicians. In another study [4], by using a paper-based microfluidic device, multiple assays are run and a camera phone is used to digitize the intensity of the color associated with each colorimetric assay. Then, the digital information from the assay site is transferred to another laboratory to be investigated by trained medical technicians.

Another proposed patient monitoring system uses a digital camera to transfer the digitized data to physicians. A wide range of rural sites cannot afford a digitizer for digitizing the radiographic images to be transferred by telemedicine to be reviewed by a physician. The feasibility of using digital cameras to take the image from the radiographic images and transmission of them through the telemedicine to the physicians has been investigated in [5]. In practice, images of 40 bone trauma cases have been transferred to a consultant center to be reviewed by two orthopedic surgeons and two radiologists. Results showed that image qualities were in the high resolution in most cases which is desirable. In another study [6], to provide the immediate medical treatment in remote areas, a telemedicine based on embedded system is proposed. In this system, biomedical signals such as blood pressure, ECG, respiration and temperature have been collected and telemonitored using general packet radio services (GPRS) technology.

Telemedicine is beneficial for both patients and doctors. Increasing the population around the world, the health-care demands are sky rocketing. Because of this increase, both waiting times in a doctor's office and treatment costs are increasing. However, using remote patient monitoring systems, physicians can diagnose an illness remotely, potentially increasing the response time and decreasing overheads include waiting time in a doctor's office. Additionally, it is difficult for the bedridden and people with disabilities to not only go to the doctor's office but also wait for assistance[7]. Remote patient monitoring systems are typically implemented using personal computers, which have high power consumption, low portability, high cost, and suboptimal performance. [7, 8]. In recent years, patient monitoring systems have also been implemented using embedded systems such as microcontrollers. In this project, we introduce Zynq system on chip device (SoC) as an effective platform for patient monitoring.

2.2 Biomedical signals

Biomedical signals enable physicians to monitor physiological activities of living organs such as protein sequences, neural and cardiac rhythm[9]. These signals are normally a function of time and described by

their amplitude, frequency, and phase. Such signals EMG, ECG and EEG, are described in this section.

2.2.1 EMG

The Electromiography (EMG) is a type of biomedical signal that measures the electrical current produced during any muscle contraction or relaxation. EMG signals are controlled by the nervous system and tied to the properties of the muscle which make EMG complicated. These signals become noisy while they are transmitted among body's tissues. Fig. 2.1, shows an EMG monitoring system which is acquiring electrical activities from the bicep.

Figure 2.1: Bicep EMG signal acquisition system

One of the important application of the EMG signals is rehabilitation of motor disabilities [10]. Two main types of EMG signal recording systems are invasive and non-invasive. Acquiring EMG signals directly from the skin needs a non-invasive sensor. This method is more noisy because the possibility of recording adjacent muscle fiber signals along with the desired muscle activities. To record more accurate EMG signals, the invasive method, which uses a needle electrode, is applied [10]. Applications include diagnosing of neuromuscular diseases, disorders of motor control and controlling the prosthetic devices such as prosthetic hand and arm. In [11], a low-cost surface EMG signal acquisition method is presented based on an Arduino microcontroller. In that workr, EMG signals are recorded from the surface of the bicep using non-invasive method. These signals are amplified, filtered and transmitted to the Arduino board for A/D conversion. The capability of a microcontroller to sample and rebuild the EMG signals has been investigated using RMS, ARV and MDF estimator. Using the EMG signals to run a prosthetic limb is considered a major advantage of EMG signals. In [12], a motor rotation system based on a muscle contraction is studied. The output of the processed data results in a pulse in each muscle contraction which could be an input to a motor for a prosthetic arm. Chapter 3, describes the EMG acquisition system in detail. In this thesis, bicep's EMG signals using non-invasive method are recorded for patient monitoring system.

2.2.2 EEG

Electroencephalography (EEG) is a method to record the brain's electrical activities. The word 'encephalography' is a combination of 'electro,' meaning electricity, and 'encephalon,' meaning the brain, and 'graph,' meaning a drawing. It is mostly non-invasive, using the electrodes attached to the scalp. Correct placement of electrodes on the scalp is critical to acquiring the desired signals. Fig. 2.2, shows EMG electrodes that are attached on a patient's scalp. Collected data is transferred to the trained physicians for monitoring.

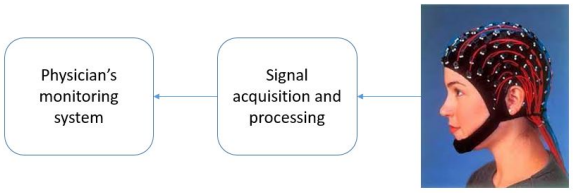

Figure 2.2: EEG-based patient monitoring

Invasive method requires an operation on the scalp for attaching the sensors into the scalp. Applications of these signals are diagnosing sleep disorders, brain death and epilepsy. The low hardware cost has made EEG an efficient option for telemedicine [13]. In [14], a telemedicine system is developed to transmit EEG signals of epileptic patient to physicians to monitor their brain activity remotely. In another study, an implementation and evaluation of a telemedicine solution for video-EEG consultation in real time, which is called tele-EEG, has been reported. This system was developed in an area in where patient had to travel to another city for EEG tests. With using this system, results from patient EEG test have been transferred to another hospital to be reviewed by trained physicians.

2.2.3 ECG

Electrocardiography (ECG) is a method to record the electrical activity of the heart during each heartbeat. Electrodes are attached to the patient's skin around the heart to collect the data. Applications such as prediction and detection of heart attacks or heart disease and monitoring the effect of heart medicines have made this method useful for telemedical applications [15]. Fig. 2.3, shows a patient who is the target of ECG monitoring.

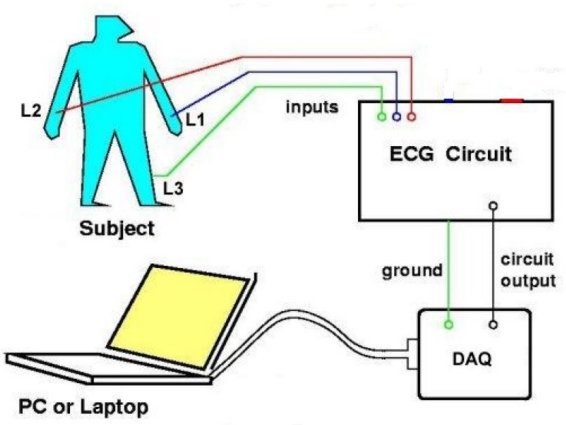

Figure 2.3: ECG-based patient monitoring

A low-cost method for real time ECG signal acquisition, which is processed in MATLAB, has been proposed in [16]. In that work, the ECG signals are sampled and digitized at 1KHz, then a microcontroller based embedded system converts the ECG data to RS232 format and transfers them into a personal computer to be processed in MATLAB. The results from the embedded system are shown on the MATLAB terminal for on-line supervision. Because a low power system i desired for the patient monitoring systems, a low-power and low-cost wireless A/D-converter (ADC) to transmit biomedical signals such as ECG has been developed in [17]. A 12-bit ADC samples the ECG data at 1KHz and sends them to the processing unit which is FPGA. A remote PC runs software to receive and process the data. Results show that the ECG signals can be transferred continuously without disruption.

2.3 Hardware acceleration

Implementation of computationally intensive algorithms in hardware, which is called hardware acceleration, increases the performance of the system compare to CPU-based software implementation systems. Computers are considered as general purpose computing systems because they are able to handle various computations. However, application specific integrated circuits (ASICs) are able to perform specific calculations much faster than the general purpose computers. Implementing some of the high computational algorithms using computer hardware, causes the system work faster compare to implementation of them only on the general purpose computer. Fig 2.4, shows the dependency between a microprocessor and a hardware accelerator.

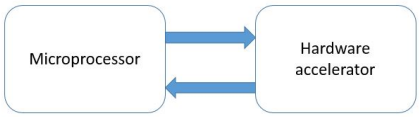

Figure 2.4: Microprocessor and hardware accelerator connection

These days, using embedded systems based on field programmable gate arrays (FPGAs), is a popular approach for hardware acceleration purposes. Using hardware accelerators has become a foundation for high performance designs. For instance, in [18], Sobel and Gaussian filters in addition to three general image processing techniques, which are average subtraction, image thresholding and image scaling, were implemented on a GPU, FPGA and two types of CPUs ATOM and ARM. The results have shown that the image size is an important factor in determining the efficiency of a platform in terms of power consumption among hardware accelerators on FPGA and software accelerators on GPU and multicore CPUs. The Zynq architecture proved to be 10 times faster performance for the images with smaller than 500×500 pixel sizes and the GPU showed 41 times higher performance for larger image sizes. Another popular application, which highly needs low power consumption and high performance, is healthcare systems. In [19], to monitor the patient rehabilitation, movements and posture of the patient require to be precisely tracked using visual and on-body sensors to determine the need for correction actions. Another example comes in autonomous unmanned aerial vehicles where data from the sensors, especially cameras, are received and need to be processed at a high frame rate [20]. The drone in that work uses a dual camera that one of them is generating 60 frame per seconds and data from the second one utilizes Sobel filter for corner detection on large images at high frame. In another work for the purpose of security [21], image processing computations are done at the camera before transmission to shrink the bandwidth of the system because only processed results are transferred which are significantly abstracted. Results showed high performance and security of this system. In [22], the performance comparison of an image convolution algorithm on GPU and FPGA has been compared. Results showed that the GPU was about 20 times faster than FPGA implementation. Similarly, the performance of FPGA, CPU and GPU for two dimensional filter and K-means clustering has been compared in [23].

Field Programmable Gate Array

Because ASICs are not configurable, they require a reliable design because once they are fabricated, the design cannot be changed. FPGAs are become more interesting for designers due to their reconfigurability yet high speed functionality. The designer is able to reprogrammed the FPGA without any cost whenever the design requires to be optimized.

The main elements in the structure of FPGAs are logic blocks. This unit consists of loock-up tables and flip-flops. To program the FPGAs, three main hardware description languages (HDL) exist, Verilog, VHDL and System Verilog. After designing a module using any of these languages, the design need to be simulated for fault detection. Riviera-pro, Active-HDL, Modelsim are some of the effective tools in this regard. Then, the design need to be synthesized using a software that is designed for that specific FPGA such as Quartus for Alter FPGAs and Vivado for Xilinx FPGAs. At the end, the FPGA is ready to be programmed.

Hardware/software co-design

Because implementing all parts of the design in hardware is difficult, specially when some of the tasks are run easier on a processor, another approach is to implement a design using both hardware and software. In this approach, some parts of the design can be implemented using software on a central processing unit (CPU) and the rest in the hardware. Selecting the potential part of the design for hardware acceleration becomes challenging in hardware/software co-design approach. It is possible to implement a microprocessor into a FPGA, which is called soft processor, and communicate with the hardware side of the chip as well. To do this, FPGA venders have their own soft processors such as Xilinx microblaze and Altera NIOS. These days, the combination of an ARM processor and FPGA into one cheap has become interesting for designers which is designed by Xilinx company.

2.4 Zynq SoC structure

These days the progression of the technology enables cutting-edge companies to encapsulate different parts of a system into a single chip, which added the System-on-Chip (SoC) concept to the electronics world. An example of SoC is the Zynq-7000 all programmable SoC family, which is the new generation of the Xilinx all programmable System-on-Chip (SoC). A Zynq device consists of two hard ARM CortexA9 processors, FPGA, ADC blocks and many other features all in one silicon chip. Before the invention of the Zynq, there were processors that were coupled with a Field Programmable Gate Array (FPGA) but in the same chip which made the communication between the Programmable Logic (PL) and Processing System (PS) complicated. The Zynq architecture as the new generation of the all programmable System-on-Chip (SoC), combines a dual-core ARM Cortex-A9 with the traditional (FPGA). The interface among parts of the Zynq architecture is based on the Advanced eXtensible Interface (AXI) standard which creates high bandwidth and low latency connection among subsystems. This interface are explained in more detail in further sections [24]. Fig. 2.5 shows an general view of the Zynq device.

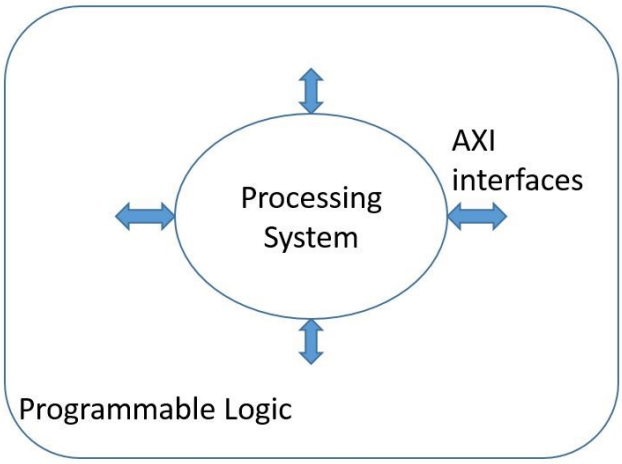

Figure 2.5: Zynq internals

A key advantage of the integrated processor and FPGA on a single chip is the ability to improve the performance of the system by accelerating the high computational functions of the design on an FPGA logic while processor is doing other tasks. Implementing softcore in FPGA brings the flexibility of processor instances into the design. However, the frequency of the ARM processor in the Zynq device can go up to 1 GHz compared to the microblaze frequency around 200 MHz. Therefore, this innovation not only brings comfort-ability and performance improvements for a user, but more significantly, by simplifying the system to a single chip, the overall cost and physical size of the device are reduced [24]. One of the main bottleneck of using hardware accelerator is exchanging data between processor and FPGA. To solve them, ARM has designed high performance interface protocols which are integrated in Zynq device[24].

In this thesis, the ARM processor makes the decision based on the results from the modules implemented in hardware. Because we have implemented image processing algorithms in hardware for the purpose of hardware acceleration, the communication between ARM and FPGA is done using AXI stream interface which is designed for streaming data. Vivado HLS tool is used to design and develop the image processin IPs. This section describes the structure of the ARM processing unit, programmable logic, AXI interfaces and communication protocols in detail.

2.4.1 Application Processing unit (APU)

The APU contains two ARM cortex-A9 processor units each of which generally includes NEON unit, floating point unit (FPU), memory management unit (MMU) and L1 caches. In addition, the APU consists of snoop control and L2 caches. Fig. 2.6, shows the structure of the APU.

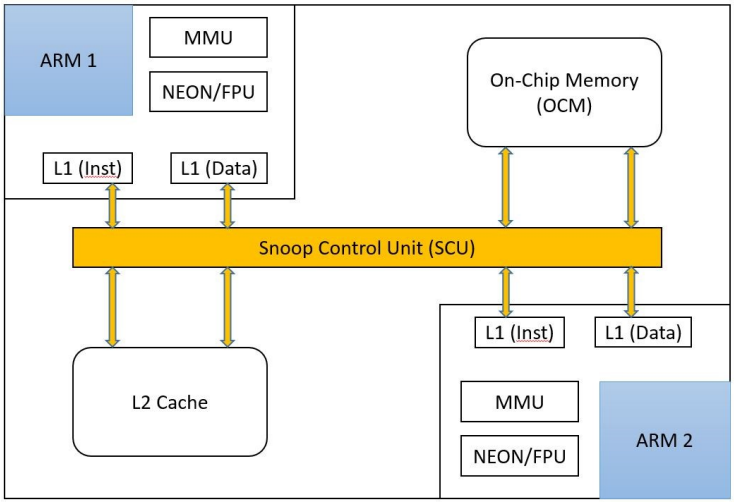

Figure 2.6: Structure of the application processing unit

The main components of the APU, which are shown in the above image, are described here:

- **NEON:**The Single Instruction Multiple Data (SIMD) is provided by this unit which brings major acceleration of DSP and media algorithms to the main ARM processor.
- **FPU:**This unit provides acceleration of the floating point operations.
- **Level 1 cache:** Each processor has its own instruction and data cache to store the instructions and data.
- **MMU:** Memory management unit translates the virtual memory addresses to the physical memory addresses.
- **SCU:** Snoop control unit controls the interfaces among processors, L1 and L2 caches.
- **L2 cache):** It is shared between the two processors that enables them to access the newest update of data.

2.4.2 Programmable logic (PL) unit structure

The programmable logic portion of the Zynq SoC consists of configurable logic blocks (CLBs) which contain two slices each of which slice contains four look-up tables (LUTs), eight Flip-flops (FFs), and an accompanying switch matrix. Additionally, Block RAMs and DSP slices exist in the PL side. Fig. 2.7, shows the structure of the PL.

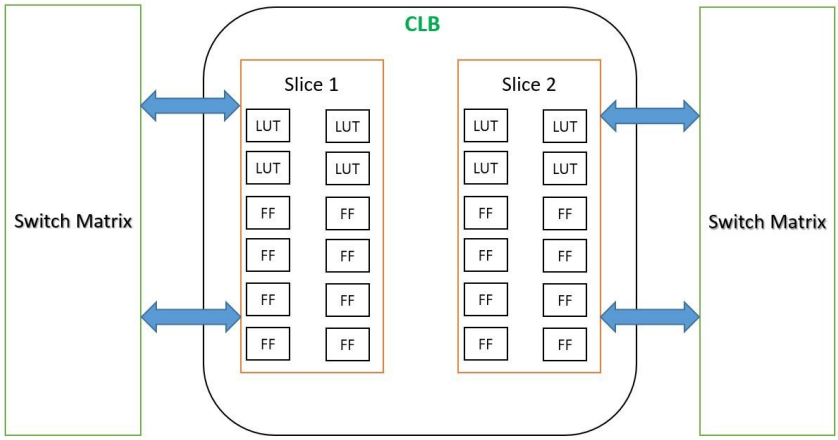

Figure 2.7: Structure of the programmable logic unit

The main components of the PL, which are shown in the above image, are described here

- **Slice:**Each slice consists of resources to implement the combinatorial and sequential circuits.
- **Look-up Table (LUT):**To implement a logic function of up to six inputs, RAM, ROM or shift registers, the LUTs are used.
- **Flip-flop (FF):** For implementation of 1-bit register with reset functionality, this sequential element is used.
- **Switch Matrix:** It provides the connection between subsystems of the inside of the CLB and also between the CLB and other parts of the PL.

2.4.3 AXI interconnection

An efficient communication protocol make receiving and transmitting data more easy. The communication among Zynq subsystems is based on AXI interconnection. The ARM Advanced Microcontroller Bus Architecture (AMBA) is an on-chip interconnection standard to connect and manage the functional blocks in a SoC design. The Advanced eXtensible Interface (AXI) is based on AMBA as a protocol for the communication among the IPs of a FPGA design [24, 25]. Here are some of the important features of an AXI interface:

- It supports burst transactions with only start address issued.
- Different phases for data and address communications exist.
- Write and read channels are separated which allows low-cost Direct Memory Access (DMA).
- Transactions can be completed out of order.

- Multiple outstanding addresses can be issued.

The hierarchy types of AXI interconnections are shown in Fig. 2.8.

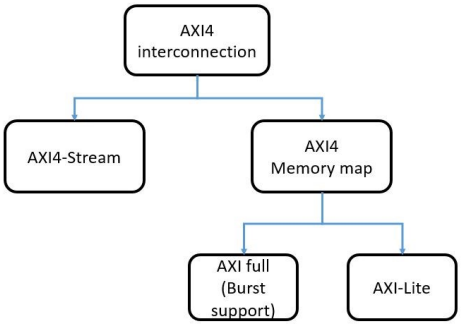

Figure 2.8: AXI4 interconnection categories

Two types of AXI4 interfaces can be used. First, the AXI4 memory map which can be further categorized into the full AXI4 and the AXI4-lite. Second, AXI4-stream which is used to stream the data in a wide range. These two are discussed in detail here. The characteristics of these AXi interface categories are as follow.

- **AXI4 memory map:** Capable of doing memory map burst transaction up to 256 data transfer cycles per address phase.
- **AXI4-Lite memory map:** Utilized for the single bit memory map transaction.
- **AXI4 stream:** There is no address channel and it allows an unlimited burst transaction between the master and slave.

The AXI write and read transaction channels are summarized into 5 categories. The important signals of each channel are described here. Fig. 2.9, shows an AXI interconnection IP and its associated ports in Xilinxs Vivado design suite.

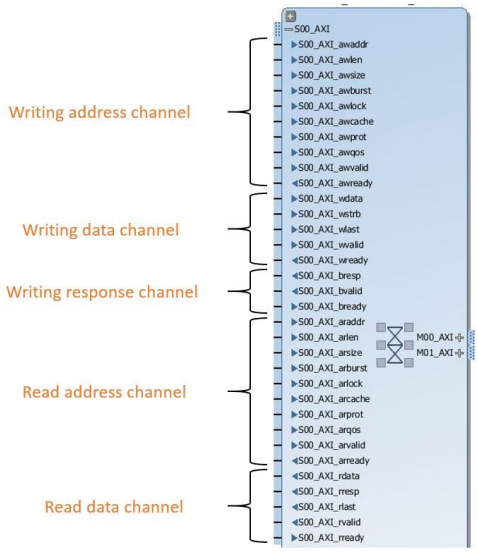

Figure 2.9: AXI interconnection IP

The communication of the master ans slave modules are done through the five main channels that are shown in the above image[25]. These processes are described below.

- **Writing address channel:** At the beginning of the transaction, the master drives the slave by sending the AWVALID which says there is a write transaction ready. After that the address to be written is sent by AWADDR to the slave. Then, the response from the slave comes through the AWREADY signal. Using AWLEN user defines the number of transfers in a burst transaction. The AWSIZE is used to clarify the size of each transaction (ex. 32 bits). Each transactions has its own ID that is sent through the AWID to the slave.

- **Writing data channel:** By the end of the the address transaction, WVALID, WREADY and WDATA signals of the writting data channel, are triggered the same as the writing address channel. The last transaction in a burst is defined through the WLAST signal. WSTRB says which bit of a bus is used for the writing transaction. WSTRB is useful when the bus is 32 bits and the data is just 2 bits.

- **Write response channel:** Used to inform the master about the status of the write transactions. BVALID is sent by slave and says that Im ready to send the response. The response from the master is sent through the BREADY. The writte response is sent through the BRESP by the slave.

- **Read address channel:** Likewise the write address channel, the ARVALID, ARADDR, ARSIZE, ARLEN, ARID and other signals are the same.

- **Read data channel:** RDATA, RID, RLAST, RVALID and RREADY work the same as the writing data channel. The status of the read transfer is identified in the RRESP.

2.4.4 PS and PL communication port

Specific ports inside the Zynq handle the communication between the PS and PL side of the Zynq. Fig. 2.10, shows the structure of these port. The direction of the arrows is from master to slave. The direction determines the master or slave characteristics of the communication port.

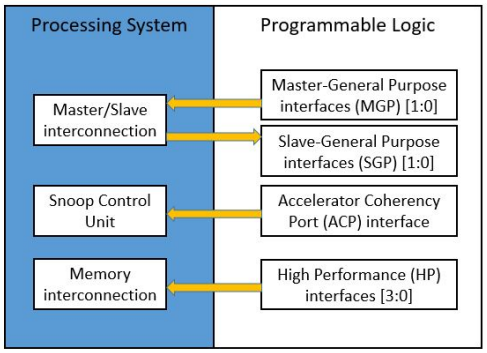

Figure 2.10: Processing system and programmable logic communication ports

As it is shown in the above image, three main communication ports exist which are described as follows: [24, 25]:

- **AXI GP:** These ports are used for the general purpose application between the PL and PS. These are the main ports for the accessing the PS to PL and vice verse.
- **High performance (HP):** These memory map connection ports provide high bandwidth data-path from the master modules in PL to the DDR memory ports or the on-chip memory (OCM) in PS.
- **Accelerator Coherency Port (ACP):** This port provides access to the memory subsystems from the PL. Through this port, the PL can also access the cache memories inside the PS which improves overall performance and power consumption.

2.4.5 Zynq design flow

The design flow of the Zynq architecture has typically four stages. The first stage is to define the specifications and requirements of the system. Second, tasks should be partitioned between PS and PL. This stage is critical because the performance of the system is increased by dividing the tasks in an efficient way. Third, the hardware/software to meet the design specification should be design. Forth, the design need to be tested and then integrated into the Zynq device. Fig. 2.11, shows the Zynq SoC design flow.

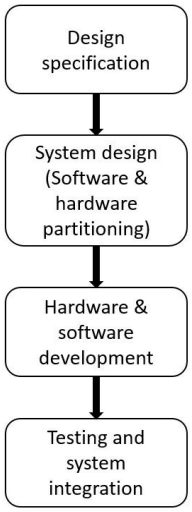

Figure 2.11: Zynq design flow hierarchy

Xilinx has provided tools for designers who use Xilinx's chips in their design [24]. In this thesis, we have used the following tools to develop the processing part of our system on the Zynq device.

- **Vivado Design Suite:** The hardware design, simulation, synthesis and implementation are done using this tool.
- **Vivado HLS:** To make the software, which is run on the PS, Xilinx Software Development Kit (SDK) is used which contains all the driver support for all the Xilinx Ips.
- **Xilinx SDK:** The Vivado High-level Synthesis (Vivado HLS) is a tool for the hardware synthesis from C-level description. This tool also used for creating IPs using high-level programming languages such as C and C++.

2.5 Image processing

Computer vision algorithms enable a computer to understand the surrounding environment using digital cameras. Using a camera and computer vision algorithms in a patient monitoring system can improve the accuracy and reliability of the system. In this section, Sobel edge detection filter, dilation, and erosion image processing algorithms are described since they have been selected for hardware acceleration purposes due to their usage in a wide range of applications. These algorithms are studied in following paragraphs.

Sobel edge detection

The Sobel edge detection filter is a computer vision algorithm which is used to create images that highlight edges. This filter calculates the gradient of the image intensity function [26]. Two operators are applied to the main image horizontally (G_x) and vertically (G_y) which can vary in size.

$$G_x = \begin{bmatrix} -1 & 0 & 1 \\ -2 & 0 & +2 \\ -1 & 0 & 1 \end{bmatrix} G_y = \begin{bmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{bmatrix}$$

In other words, the edge detection algorithms detect sharp changes in the brightness of an image. This enables us to detect changes in the object orientation, changes in the material used in the image, variations in scene illumination and discontinues in depth. In a patient monitoring system, to monitor the posture of a patient edge detection algorithms are used. It is also used to detect edges in a radiographic image.

Dilation

Dilation is a computer vision algorithm that creates an image with the same shape as the original image, but in different size. This operation $A \oplus S$ gets a binary image as an input and increases the size of the connected components. The size and shape of the structuring element defines the amount of growth in the edges. This process is done by adding pixels to the edges which may cause the edges seem wider [27].

$$A \oplus S = z \mid (S_z) \cap A \neq \Phi$$

where, A is the original image, S is the structuring element and z is displacements (x,y) locations

Erosion

Erosion is a computer visoon algorithm which erodes away undesired boundaries of the image. This operation $A \ominus S$ receives a binary image as an input and erodes it. The erosion amount depends on the shape and size of the structuring operator. By applying this element on the image, some of the pixels are removed from the edges of an object which may caused the edges to seem thinner [27].

$$A \ominus S = \ z \mid (S_z) \subseteq A$$

where,A is the original image, S is the structuring element, and z is displacements (x,y) locations.

Chapter 3

Methodology

In this chapter, we present our design, development and testing of the EMG-based patient monitoring system using Zynq SoC device. This system consists of four main blocks as shown in Fig. 3.1. The process of recording the EMG signal from the patient's skin are encapsulated into the EMG signal acquisition block. The acquired signals are noisy and low-amplitude and the signal conditioning block filters and amplifies them. These amplified signals are then analyzed and processed. The system also includes a camera that sends visual information of the patient to the processing system. The Zynq device is used in this project as the Processing Unit because of having an ARM dual core cortex-A9 as well as an FPGA integrated on a single chip.

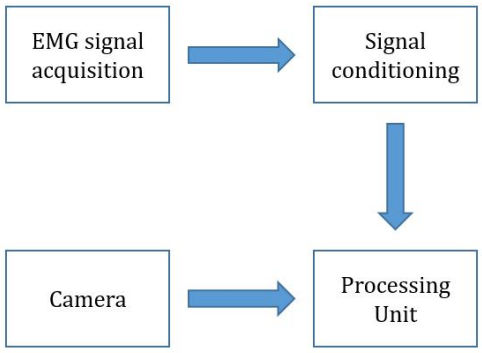

Figure 3.1: Zynq-based patient monitoring system block diagram

Fig. 3.2, show A more detailed view of the developed system. The top left of the image shows the patient EMG signal acquisition process. First, the brain's motor cortex generates the commands for any muscle contraction. These commands are transmitted into the muscle motor neurons and cause muscle contraction.

EMG sensors capture the electrical activity of the desired muscle. For amplification and filtering processes, these signals are sent to a preamplifier, low-pass filter, high-pass filter and a differential amplifier. Amplification and filtering circuits are designed based on the amplitude and frequency of the EMG signals. Then, these signals need to be digitized for digital signal processing.

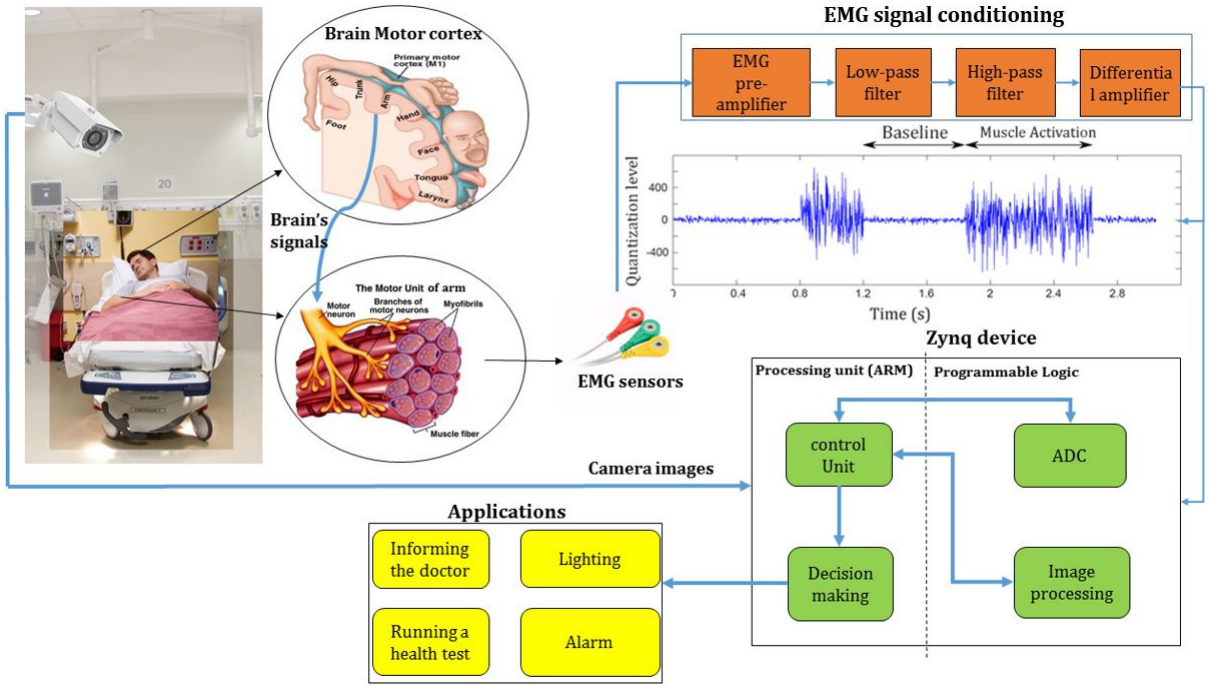

Figure 3.2: An overview of the developed system

The Zynq device handles all the data processing tasks. The analog-to-digital converter (ADC) digitizes the recorded EMG signals and sends them to the processor for decision making processes. Meanwhile, an image from the patien's body is sent to the Zynq device to be processed based on three different image processing applications, Sobel edge detection, dilation, and erosion. The "application" block in the image shows the potential applications that can be done using processed data. In this project, the lighting application is developed.

This chapter describes every parts of the above image in detail. In this project, Sobel edge detection, dilation, and erosion image processing algorithms are also implemented in a PC-based system using MATLAB and OpenCV. This chapter also describes this PC-based implementation. Because one of the advantages of implementing computationally intensive algorithms in hardware is achieving low power consumption, our method to analyze the power performance of the Zynq based and PC-based implementation is proposed at

the end of this chapter.

3.1 EMG signal acquisition

This section discusses the preparation steps before recording the EMG signals including skin noise elimination, electrode-noise reduction, electrode placement and routing. For muscle activities, the brain sends the controlling command generated in motor cortex layer through an electrical signal to the motor unit of the arm and it responds to the request accordingly. For example, thousands of commands need to be sent by the brain to lift a glass of water. The amplitude of the EMG signals vary between 1 to 10 mV. Signals lie in the frequency range between 0 to 500 Hz in which the critical signals are between 50 to 150 Hz. EMG signals are highly affected by noise and these noises mostly caused by sources including power supply, electromagnetic radiations such as radio transmission devices and fluorescent lights. These noises can be caused also by inappropriate sensor selection, wrong sensor placement, high impedance wires and motion artifacts [28, 29]. Following paragraphs discusses preparation processes to eliminate these noises.

3.1.1 Skin noise elimination

The impedance balance between the electrode and skin helps to reduce the noises caused by electrode and skin. A general rule would be having lower impedance in both sides, electrode and skin. Examples of important skin factors that caused increase in impedance are dead cells and oil. Because in this project, EMG signals have captured from the bicep, the user's bicep has been cleaned by alcohol before signal capturing to remove the skin's oil and dead cells. Moreover, "Signa Gel" has been used to increase the conductivity of the skin [30, 31].

3.1.2 Electrode-noise reduction

Factors such as shape, size, and sensor's material can create noise in the system if they are selected inappropriately. Sensors are often in circular, square and bar shape. According to SENIAM (Surface ElectroMyoGraphy for the Non-Invasive Assessment of Muscles), the main influencing factor for selecting electrodes is having identical surface area. Applying this factor caused the system to have similar input impedance at each electrode. The conductive area of the electrode is considered as the size of the electrode. SENIAM recommends that maximum size of the electrode in the direction of the muscle is 10mm. They have shown that circular electrode with the diameter of 10mm is an efficient choice. Regarding the material, SENIAM recommends the pre-gelled Ag/AgCl which is Silver or Silver Chloride. Using gold as the electrode material is a better choice because of high conductivity, however, the price is challenging [32]. In this thesis, the "Muscle Sensor Surface EMG Electrodes - H124SG Covidien" constructed by [33]. Fig. 3.3 , shows the structure of this sensor. This sensor meets the mentioned requirements.

Figure 3.3: EMG electrode

3.1.3 Electrode placement and routing

As the EMG signals provide a view of muscle activities in the body during muscle contraction, the placement of the electrodes should be consistent across recording sessions. Correct EMG sensor placement is critical to achieve high resolution signals which are appropriate for data extraction. Three types of configuration of sensor placement are monopolar, bipolar and multipolar which are explained in followings.

The monopolar configuration is implemented using a sensor to collect the EMG signals and a reference sensor. This method is used because of its simplicity. However, it is not recommended for precise acquisition. Second, bipolar configuration which is a method for acquiring surface EMG signals using two electrodes. In this method, to capture EMG signals, each muscle requires three sensors called reference, positive and negative. It is recommended to place the positive and negative surface EMG electrodes between the tendons insertion and the motor unit of the muscle, along the longitudinal mid-line of the muscle [34]. The distance between the center of positive and negative electrodes should be 1-2 cm to acquire high resolution signals. Also, the longitudinal axis of the electrodes should be parallel to the length of the muscle fibers. All the signals from positive and negative sensors are collected with respect to a reference. This electrode plays the ground rule for the system. The reference electrode needs to be attached in a place far from the other electrodes without any muscle. To do this, placing the electrode on a bone such as elbow is a good choice. The last method is multipolar configuration. This method uses more that two sensors for signal acquisition. This method causes crosstalk and noise reduction. This method is often used in comprehensive study of EMG muscle fiber orientation and motor point localization. In this thesis, the bipolar configuration has been used to acquire EMG signals [28, 32].

The placement of the electrode on the muscle affects the resolution of the recorded data. The motor unit of the muscle used to be considered as the appropriate place for sensor attachment. However, these days it is considered as the worst place for recording the signals from the muscle contractions because of lack of

EMG signal resolution with low amplitude [34]. In this regard, the electrodes should not be attached either close to the tendon or at the edge of the muscles. The placed sensors on the edge of the muscles increase the chance of interfering signals from nearby muscle which results in imprecise signals. Fig. 3.4, shows the mentioned place on the bicep for electrode attachment.

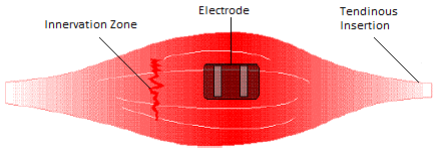

Figure 3.4: Correct electrode attachment

Quality of the materials that is used in the sensor's wires can change the conductivity of the wire which ends up with recording low resolution EMG signals. Choosing a low impedance wire causes the signals to be noise secured. Fig. 3.5, shows the wire which is used in this project which is designed and produced by Bio-medical company.

Figure 3.5: Applied wire for transferring electrode signals to EMG acquisition circuit

3.2 Signal conditioning system

Because the acquired signals are noisy and low amplitude (1 - 10 mV), the signal conditioning circuit filters and amplifies the recorded EMG signals for further analysis. The critical frequency of the bicep's EMG signals, which are between 50 to 150 Hz, are filtered using an active low-pass and high-pass filter. This section describes the process of designing the signal conditioning circuit developed for this thesis. This circuit

consists of pre-amplifier, low-pass filter, high-pass filter and differential amplifier stages [32]. Fig. 3.6 shows the designed analog circuit.

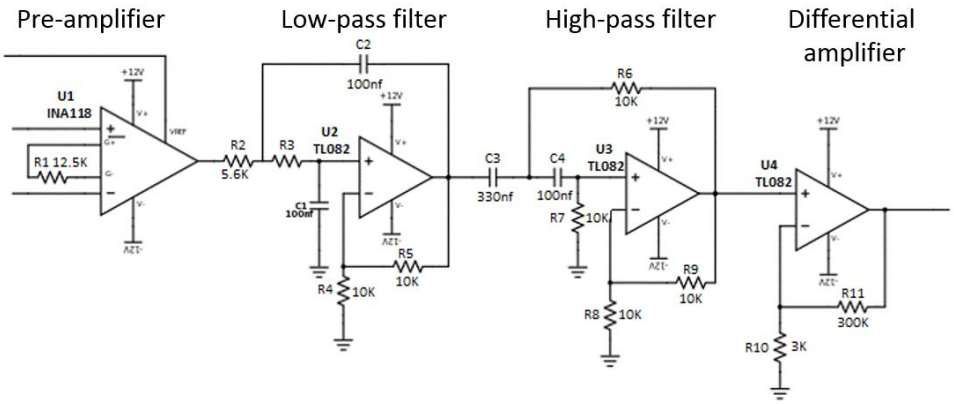

Figure 3.6: EMG signal acquisition circuit

3.2.1 Pre-amplifier

Because the amplitude of the surface EMG signals are low (1 - 10 mV), we need to amplify them before doing other processes. The quality of the EMG signals highly depends on the characteristics of the pre-amplification stage. The pre-amplifier receives two input signals, subtracts and multiplies them by the desirable gain. Characteristics of an efficient pre-amplifier are as follows [32]:

- **High input impedance**: In order to measure a signal accurately, the input resistance of the measurement device should be larger than the impedance of the sensor and skin to collect all the signals, unless signals are distorted.
- **High common mode rejection ratio (CMRR)**: The differential amplifier subtracts the signals coming from positive and negative electrodes which causes noise elimination because common signal components are ignored from the signals. This criteria is achieved by having a high CMRR.
- **Low DC offset**: Skin impedance and the chemical reaction between electrode and skin create DC voltages. These DC voltages should not be amplified because they cause the pre-amplifier to be saturated and unstable. Therefore, the ideal pre-amplifier is desired to have an inconsiderable low DC offset.

In medical measurements, instrumentation amplifiers are mostly used for pre-amplification. This amplifier includes all of the criteria mentioned above about the ideal pre-amplifier [35]. An instrumentation amplifier is composed of three differential amplifiers. Two of them are designed to work as a buffer to each

input voltage and the other one creates desired output [36]. Fig. 3.7, shows the structure of an instrumentation amplifier. The output gain of the amplifier is determined by R_g resistor.

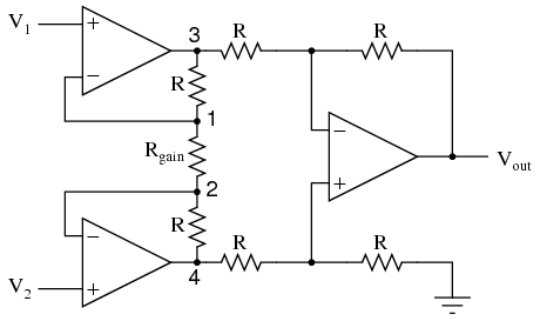

Figure 3.7: Structure of an instrumentation amplifier

In this project, INA118 instrumentation amplifier is used for the pre-amplification stage because of high accuracy and trusty results in medical measurements. The gain for this amplifier has been designed as 5. We chose the pre-amplification gain a small (5) because of preventing the amplification of undesired frequency which are going to be filtered in the next stage. To achieve this gain (5), R_g need to be selected as 12.5KΩ. Therefore, the output of the pre-amplifier would be:

$$V_o = 5(V2 - V1).$$

where V_2 is the positive EMG signal and V_1 is the negative one. Fig. 3.8, shows the schematic of the designed pre-amplification stage.

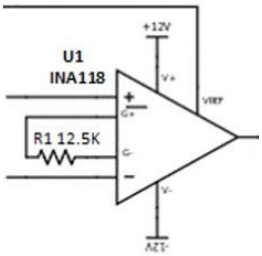

Figure 3.8: Second order active low-pass filter

3.2.2 Low pass filter

As described earlier, the recorded frequency of EMG signals are between 10 to 500 Hz in which the frequencies between 50 to 150 Hz are mostly important. To cut all the signals above the 150 Hz a second order

active low-pass filter with the cut-off frequency of 150Hz is designed. However, in practice, the exact cut-off frequency is around 172 Hz because of the tolerance of the capacitors and resistors used in the design[37, 35]. Fig. 3.9, shows the developed low-pass filter. This low-pass filter is designed based on the Sallen-Key architecture using TL082 operational amplifier[38].

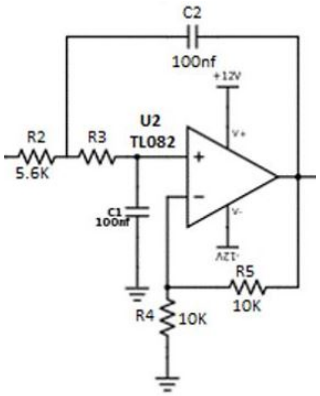

Figure 3.9: Second order active low-pass filter

3.2.3 High pass filter

To cut the frequencies under 50 Hz, a high-pass filter is designed and implemented with the cut-off frequency of 50 Hz. A second order active high-pass filter is designed for better precision. In practice, The cut-off frequency is about 70 Hz because of the tolerance of used passive components [37]. Fig. 3.10, shows the developed high-pass filter. This high-pass filter is designed based on the Sallen-Key architecture using TL082 operational amplifier.

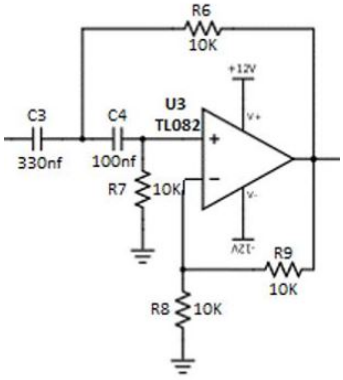

Figure 3.10: Second order active high-pass filter

3.2.4 Differential amplifier

As of now, the signals are pre-amplified and filtered for noise reduction. Even after the pre-amplification stage, the amplitude of the signals are still in a low range (5 - 50 mv). For further processing, a non-inverting differential amplifier is required to transfer the EMG signals into the voltage level. To do this, a differential amplifier with the gain of 100 is designed as the last stage of the signal conditioning circuit [35]. Fig. 3.11, shows the developed differential amplifier using TL082 operational amplifier.

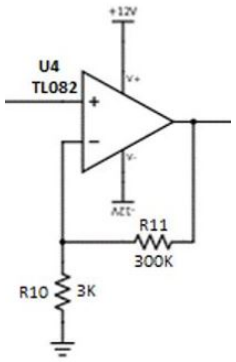

Figure 3.11: Second order active high-pass filter

3.3 Processing setup

Because the recorded EMG signals are analog, they need to be digitized for any digital signal processing. A Zynq-based embedded system board is used to digitize and process the EMG signals. In this section, components in conjunction with the Zynq-based system are described.

3.3.1 TySOM-1-7Z030 evaluation board

In this project, the TySOM-1-7Z030 evaluation board is used as a Zynq-based development board which is designed and created by Aldec Inc [39]. This board has various peripherals such as USB 3.0 and 2.0, HDMI, sim card, LCD connectors, Ethernet, mini-PCIe and etc. It also has an GTX line which can support high performance communication with external devices with up to 12.5 GB/sec. Implementing all of mentioned interface in a compact size as well as great technical support, helped us a lot to complete this thesis. Fig. 3.12 shows TySOM-1-7Z030 evaluation board.

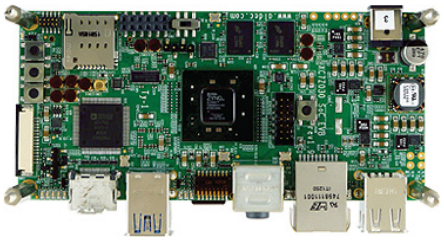

Figure 3.12: TySOM-1-7Z030 evaluation board

As it was mentioned before, Zynq device consists of two built-in ARM processors and FPGA. Having utilized both ARM processor and FPGA sides of this device provide an efficient results for Zynq users. In this project, ARM processor controls the inside and outside interfaces and FPGA handles the computationally intensive image processing algorithms, ADC and memory access tasks.

3.3.2 ARM dual cortex A9 processor

ARM processor configures the implemented hardware in FPGA at first. As this configuration does not need burst transactions, it is typically done using AXI-Lite interface. ARM processor is also responsible for decision making. When an IP finishes its task, the ARM processor receives the output of the IP and makes the output decision based on them. In this project, ARM processor configures the ADC block and keeps reading the digitized EMG signals. As soon as it detects any digital signal that corresponds with 1.2 V, an image from the patient's body, which is stored in the DRAM, is sent to the image processing IP that is implemented in the FPGA. The ARM processor reads the processed data and makes the decision based on them. In this project, blinking an LED is the last decision made by the ARM core. Fig. 3.13 shows the flowchart of the processing stages that described here.

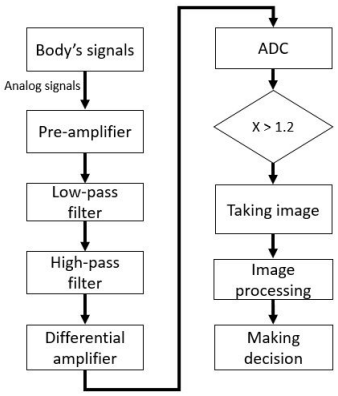

Figure 3.13: Flowchart view of the developed system

3.3.3 Analog to digital conversion (ADC) module

The Xilinx Zynq-7000 family device contains a built-in ADC which can be used for digitizing the internal sensor data and external analog inputs. This unit is called the XADC which stands for Xilinx Analog to digital converter and enables analog mixed signal functionality on the Zynq device. The XADC consists of a dual 12-bit, 1 mega sample per second (MSPS) ADC and on chip sensors [40]. In this project, the amplified EMG signals are transferred into the Zynq device through the XADC dedicated input pins which exist on the TySOM-1-7Z030 board. This unit digitizes the input signals and sends them to the ARM processor for further processing. Fig. 3.14, shows the EMG signal acquisition circuit connected to the XADC Using TySOM-1-Z7030 evaluation board.

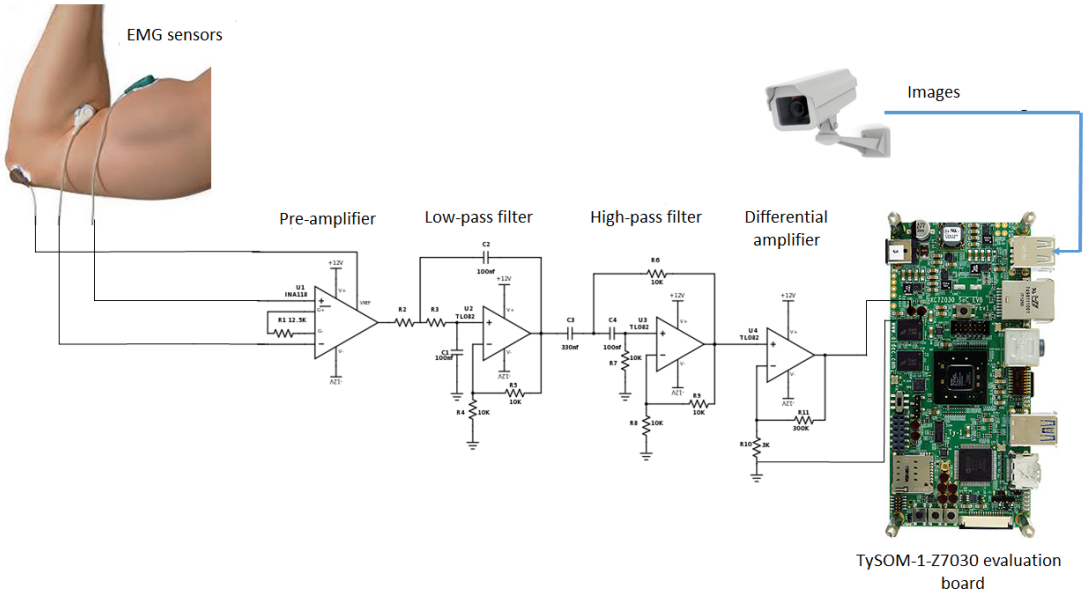

Figure 3.14: Interface between acquired EMG signals and XADC

3.3.4 Direct Memory Access (DMA) module

The AXI stream protocol becomes handy when the project is more focused on the data flow and is not involved with the memory. As an example, any image processing soft IP, which needs to send and receive image frames from each other, uses AXI stream protocol to speed up the communication. The DMA IP provides high-bandwidth direct memory access between the memory and any AXI stream interface IP. This IP supports the data bandwidth up to 1024 bits on an AXI stream interface. To make the interface between any AXI4 stream IP with the memory, DMA translates AXI4 stream data into memory map and vise verse [41]. In this project, after detecting any muscle contraction, the DMA reads the image from the memory and translate it into AXI stream protocol , which is understandable for AXI stream based IPs, and sends the data to the image processing IP. Then, it receives the processed data and translate them into AXI memory map interface to be stored in the DRAM. Using the DMA IP into the Zynq designs, the time consuming process of accessing the memory by ARM processor is omitted. In this project, the ARM processor is not included in memory accessing processes and all of them are done in the hardware side.

3.3.5 Timer module

A timer records the time while image processing IP is processing the images. This IP implemented in FPGA and counts the number of clock cycles required to complete the image processing algorithm. By having the period of each clock cycle, the timer IP calculated the spent time. In this project, the recorded time for each of the Sobel edge detection, dilation, and erosion algorithms are compared with the PC-based implementation

of these algorithms in Chapter 4.

3.3.6 Sobel edge detection, dilation, and erosion modules

In this project, basic morphological operations including erosion and dilation, which are used in most of the image processing algorithms, are implemented into the hardware. In addition, the Sobel edge detection filter, which is used for object detection, is also implemented to the hardware. These IPs are created using Vivado HLS tool. This tool uses OpenCV library and enables us to create image processing IPs. These IPs receive the input image and transfer the output image through the AXI stream interface. The image is transform into the matrix view before the filter element is applied on it. In this thesis, Sobel edge detection uses an 5×5 element and dilation and erosion use a 3×3 element. After image processing, the output data is changed to the AXI stream format to be transferred through AXI stream interface to the DMA.

The implemented IPs and their communication interfaces are shown in Fig. 3.15. The processing unit, programmable logic unit and the memory unit are separated for clarity. The amplified EMG analog signals are entered to the XADC from the top right of the image. The AXI timer IP measures the performance by counting the execution time for image processing applications. The AXI GPIO IP provides the connection between Zynq and the on-board LEDs. The processing unit interacts with XADC, timer and GPIO IPs through the AXI GP communication port. The AXI GP and AXI HP, which were described in Chapter 2.4.4, are used for PS and PL communications. As it is shown, the DMA is connected to the memory unit through the AXI HP protocol.

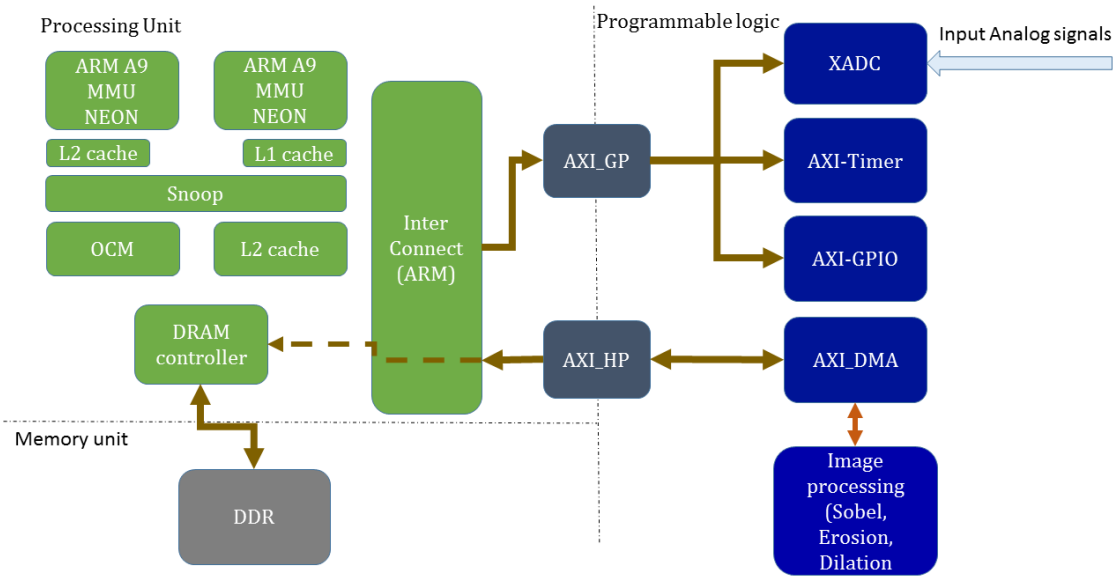

Figure 3.15: Zynq block diagram

These IPs are implemented into the Zynq device using Vivado design suite tool version 2015.02. This tool has a feature to demonstrate the design block IP diagram. Fig. 3.16, shows this block diagram made by Vivado Design Suite tool.

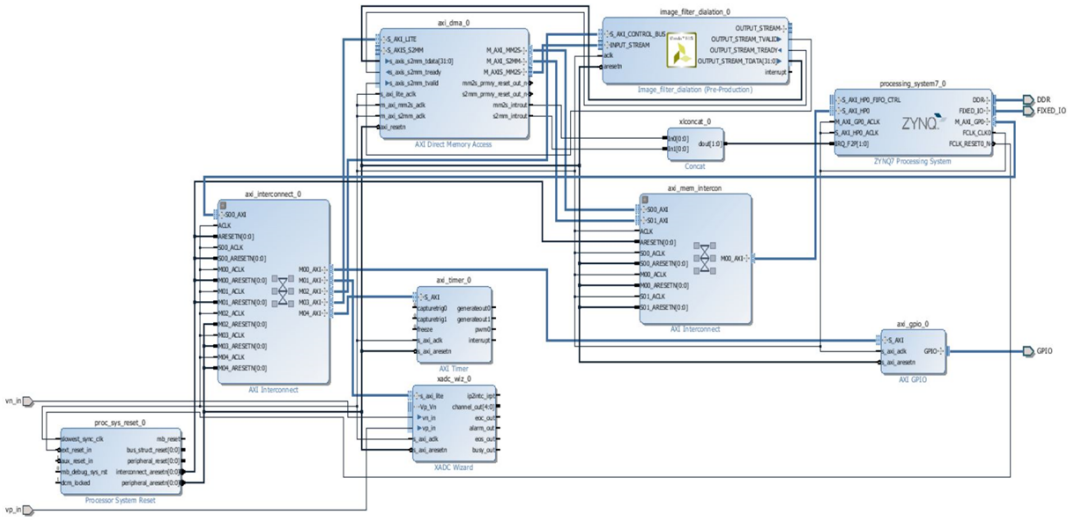

Figure 3.16: Complete project block design by Vivado

3.4 Applications

In this project, in addition to the image processing applications, a LED blinks as soon as desired EMG signals are detected. This application is selected because of its potential to be considered as various applications. For instance, if we consider the LED as a switch, this application can be configured as sending a health status to the patient's physician, turning on an alarm in the case of emergency and showing massages from the patient's physicians on an LCD. In this project, lighting the patient's room as soon as the camera wants to take a picture or shoot a video of the patient is considered as the main goal for this application. In this case, the room has enough luminance to capture desirable images.

3.5 CPU-based implementation

CPU-based systems are called general purpose processors as they are not limited to compute some specific applications. Because in patient monitoring systems specific tasks are assigned to the processing unit, existing patient monitoring systems are implemented using embedded systems which are designed for specific tasks. In this project, in addition to the design the system on the Zynq SoC device, implementation of image processing algorithms is also done using a PC for analyzing the comparison to the Zynq device. Image processing applications on a PC are built typicaly using MATLAB, or the OpenCV library. In this project, we first implement the Sobel edge detection filter, dilation, and erosion image processing algorithms using MATLAB. MATLAB uses interpreter, which runs the code line by line and the complier runs all at the same time, while the OpenCV library needs a C++ compiler. Thus, MATLAB is typically slower than OpenCV. In this regard, we also implement the mentioned image processing algorithms using the OpenCV library in Microsoft Visual Basic. Results of mentioned implementation are discussed in Chapter. In this project, a PC with the following configuration is used to implement the mentioned application. It is made by lenovo and consists of a 3.4 GHz Intel Core-i7 CPU, 8 GB memory with the windows 7, 64-bit operation system. Results of the image processing implementation on both Zynq-based and PC-based system are introduced in Chapter 4.

3.6 Power performance analysis

One of the advantages of implementing the high computationally demanding algorithms on an FPGA is achieving low power consumption. The reason behind this fact is that FPGAs are application specific systems and use only necessary modules for data processing. For instance, while a microprocessor works, subsystems including Arithmetic Logic Unit (ALU), Memory Management Unit (MMU) consume power even if they are not in used. However, in FPGA, all the required modules in a design are implemented by the designer. In this section, we measure the power consumption of the TySOM-1-Z7030 evaluation board and the PC-based system while running image processing algorithms. To do this, the "Watt's Up meter" device, which is a product of RC electronics Inc, has been used [42] for measuring the power of Zynq-based

system. One side of this device is connected to the power supply and the other side of that is connected to the load which is the TySOM-1-Z7030 evaluation board. Fig. 3.17, shows the Watts' Wp meter connected to the board.

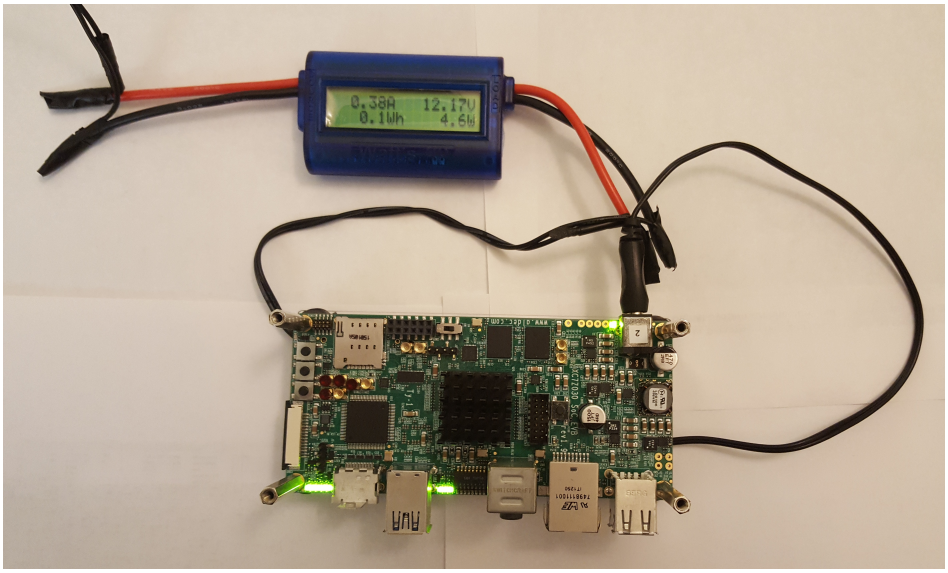

Figure 3.17: Watt's Up meter connection to the TySOM-1-Z7030 board

Because the Watts' Up meter cannot measure AC Voltages, to measure the power consumption of the PC-based based system, Kill a Watt device from P3 international company is used [43]. Fig. 3.18, shows the Kill a Watt device. Results of power comparisons are discussed in Chapter 4.

Figure 3.18: Kill a Watt meter connection to the TySOM-1-Z7030 board

Chapter 4

Results and Discussion

This chapter discusses the results of implementing the Sobel edge detection filter, dilation, and erosion image processing algorithms on both Zynq-based device and PC-based system.

4.1 Image processing algorithms using Zynq device

To discuss the performance of the hardware implementation, Sobel edge detection filter, dilation, and erosion algorithms have been implemented into the FPGA. As soon as detecting the desired EMG signal, A 60×60 image is transferred into the FPGA to be processed using implemented image processing IPs. Because we want to compute the performance of the image processing IP implemented in the hardware, the system is not designed as real time and DMA sends the image and receives the processed data from the IP one time. Meanwhile, a timer module records the execution time of the hardware implementation. One of the major advantages of using FPGA is reconfigureability. This advantage enables us to achieve different performances by configuring the FPGA in different clock frequencies. In the Zynq device, the maximum clock frequency that the programmable logic supports is 250MHz. With respect to this range, we choose 30, 50, 100, 150 MHz and the maximum frequency that the design can support. The maximum frequency is calculated based on critical path of the circuit which creates the most delay in the circuit. The Sobel edge detection filter, dilation, and erosion image processing algorithms are implemented and tested into the hardware using mentioned frequencies. Table 4.1, shows results of implementing the Sobel edge detection filter, dilation and erosion image processing algorithms in hardware. We calculated the execution time as the average performance of 30 trials on each algorithm.

Table 4.1: Execution time of the Zynq-based implementation

Clock frequency (MHz)	Sobel (us)	Dilation (us)	Erosion
30	122.4	120.2	121.1
50	73.6	72.6	72.8
100	37.1	36.4	36.3
150	25.7	24.2	24.2
Max Freq*	20.9	17.7	17.3

* The maximum frequency for Sobel, dilation and erosion are 187, 205 and 208 MHz respectively.

4.2 Image processing algorithms using personal computer

In this thesis, we also implemented the computationally demanding image processing algorithms using MATLAB and OpenCV on a personal computer. Table 4.2, shows the performance of the image processing algorithms implementation in the PC using MATLAB and OpenCV in Microsoft Visual Basic. We calculated the execution time as the average performance of 30 trials on each algorithm.

Table 4.2: MATLAB execution time

Algorithms	Sobel	Dilation	Erosion
Matlab	38.1 (ms)	32.5 (ms)	34.3 (ms)
OpenCV	846.2 (us)	823.1 (us)	821.3 (us)
Speed up	45	39	41

As shown in the above table, implementation of the Sobel filter, dilation and erosion algorithms in OpenCV are 45, 39 and 41 times respectively faster than MATLAB. As it is shown in the table, OpenCV execution time is much faster than MATLAB because it is written in C++ language which is closer to the hardware language than MATLAB's scripts.

4.3 Comparison of the Zynq and PC-based system performances

Results of the OpenCV, MATLAB and Zynq device implementation are compared here. The Zynq FPGA execution time that corresponds to maximum frequency has been selected for performance comparison. Results show that implementation of Sobel edge detection, dilation, and erosion image processing algorithms in hardware are 40, 47 and 47 times faster than PC-based implementation. Results of the Zynq implementation are also about 1822, 1836 and 1982 times faster than the MATLAB implementation. Table 4.3 compares the performance of the OpenCV, MATLAB and Zynq implementation together.

Table 4.3: Zynq and OpenCV comparison

Algorithms	Sobel	Dilation	Erosion
OpenCV	846.2 (us)	823.1(us)	821.3(us)
Matlab	38.1 (ms)	32.5 (ms)	34.3 (ms)
Zynq	20.9(us)	17.7(us)	17.3(us)
Speed up over OpenCV	40	47	47
Speed up over MATLAB	1822	1836	1982

4.4 Power consumption analysis

One main advantages of the hardware implementation is achieving lower power consumption. The watt meters used in this thesis showed that TySOM-1-7Z030 evaluation board, which is based on Zynq device and used PC consumes 5.9W and 30.3W respectively, on average. Results of the running image processing algoritnms using MATLAB showed that PC consumes 45.2W which is about 15W over its average power consumption. Results of the running image processing algorithms using OpenCV showed that the PC consumes 39.3W which is about 9W more than its average power consumption. Running the image processing algorithms using Zynq system showed that it consumes 7.1W which is about 1W more than its average power consumption. Consequently, Zynq device consumes 6.3 times less than the PC while using MATLAB and 5.5 times less than PC while using OenCV. Table 4.4, shows the results of the PC and Zynq device power consumption while processing the image processing algorithms.

Table 4.4: Power consumption comparison

Application	Power consumption
PC-MATLAB	45.2 (W)
PC-OpenCV	39.3 (W)
Zynq Device	7.1 (W)
Zynq / PC-MATLAB	6.3
Zynq / PC-OpenCv	5.5

Chapter 5

Conclusion and Future Work

In this thesis, we designed, developed and tested an EMG based patient monitoring system using Zynq SoC device. In this project, with detection of a desired EMG signal from the patient's body, an image of the patient is transferred to the FPGA side of the Zynq device for image processing algorithms. Sobel edge detection filter, dilation, and erosion image processing algorithms are implemented into the FPGA for hardware acceleration purposes. As an application, a LED starts to blink, which corresponds to lighting the patient's room, as soon as the desired EMG signal is detected. We also the performance of the image processing algorithms in hardware to a PC-based system using MATLAB and OpenCV. Results showed that the performance of the Sobel edge detection, dilation, and erosion image processing algorithms on the Zynq device are 1822, 1836 and 1982 times faster respectively than PC-based system using MATLAB. Results also showed that the mentioned image processing algorithms on the Zynq device are 40, 47 and 47 times faster respectively than PC-based system using OpenCV. Additionally, the power consumption of the developed system was compared to the PC-based system. Results showed that the PC-based system consumes 45.2W and 39.3W when the image processing algorithms are processed using MATLAB and OpenCV, respectively. The Zynq device consumes 7.1W while running the image processing algorithms. By increasing the demand of using one or multiple cameras in the patient monitoring systems, the processing units need to be high performance and low power. Results of this thesis showed that developing a patient monitoring system using Zynq SoC device outperforms the PC-based systems. For future studies, we plan to develop a real-time EMG based patient monitoring system in which a real time video of the patient is processed in the Zynq device. Moreover, extra sensors such as blood pressure, blood glucose and heart beats will be attached to the patient's body to monitor the health status and send the collected data to a server.

Bibliography

[1] P. A. Mou, C. H. Chen, S. H. Pun, P. U. Mak, and M. I. Vai, "Portable intelligent bioelectric signals acquisition system with an adaptive frontend implemented using fpga and fpaa," in *World Congress on Medical Physics and Biomedical Engineering, September 7-12, 2009, Munich, Germany.* Springer, 2009, pp. 348–351.

[2] S. Pavlopoulos, E. Kyriacou, A. Berler, S. Dembeyiotis, and D. Koutsouris, "A novel emergency telemedicine system based on wireless communication technology-ambulance," *IEEE Transactions on Information Technology in Biomedicine*, vol. 2, no. 4, pp. 261–267, 1998.

[3] C. Lau, R. S. Churchill, J. Kim, F. A. Matsen, and Y. Kim, "Asynchronous web-based patient-centered home telemedicine system," *IEEE Transactions on Biomedical Engineering*, vol. 49, no. 12, pp. 1452–1462, 2002.

[4] A. W. Martinez, S. T. Phillips, E. Carrilho, S. W. Thomas III, H. Sindi, and G. M. Whitesides, "Simple telemedicine for developing regions: camera phones and paper-based microfluidic devices for real-time, off-site diagnosis," *Analytical chemistry*, vol. 80, no. 10, pp. 3699–3707, 2008.

[5] E. Krupinski, M. Gonzales, C. Gonzales, and R. S. Weinstein, "Evaluation of a digital camera for acquiring radiographic images for telemedicine applications," *Telemedicine Journal and e-Health*, vol. 6, no. 3, pp. 297–302, 2000.

[6] W. Ping, W. Jin-gang, S. Xiao-bo, and H. Wei, "The research of telemedicine system based on embedded computer," in *2005 IEEE Engineering in Medicine and Biology 27th Annual Conference.* IEEE, 2006, pp. 114–117.

[7] Y. Mori, M. Yamauchi, and K. Kaneko, "Design and implementation of the vital sign box for home healthcare," in *Information Technology Applications in Biomedicine, 2000. Proceedings. 2000 IEEE EMBS International Conference on.* IEEE, 2000, pp. 104–109.

[8] A. I. Hernandez, F. Mora, M. Villegas, G. Passariello, and G. Carrault, "Real-time ecg transmission via internet for nonclinical applications," *IEEE Transactions on Information Technology in Biomedicine*, vol. 5, no. 3, pp. 253–257, 2001.

[9] M. Akay, *Biomedical signal processing.* Academic Press, 2012.

[10] M. Reaz, M. Hussain, and F. Mohd-Yasin, "Techniques of emg signal analysis: detection, processing, classification and applications (correction)," *Biological procedures online*, vol. 8, no. 1, pp. 163–163, 2006.

[11] I. L. B. de Moura, L. C. d. S. M. Ozelim, and F. A. Soares, "Low cost surface electromyographic signal amplifier based on arduino microcontroller," *World Academy of Science, Engineering and Technology, International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering*, vol. 8, no. 2, pp. 303–307, 2014.

[12] S. Sudarsan, I. Student Member, and E. C. Sekaran, "Design and development of emg controlled prosthetics limb," *Procedia Engineering*, vol. 38, pp. 3547–3551, 2012.

[13] D. P. Subha, P. K. Joseph, R. Acharya, and C. M. Lim, "Eeg signal analysis: a survey," *Journal of medical systems*, vol. 34, no. 2, pp. 195–212, 2010.

[14] F. Vaz, O. Pacheco, and A. M. da Silva, "A telemedicine application for eeg signal transmission," in *Engineering in Medicine and Biology Society, 1991. Vol. 13: 1991., Proceedings of the Annual International Conference of the IEEE.* IEEE, 1991, pp. 466–467.

[15] S. Karpagachelvi, M. Arthanari, and M. Sivakumar, "Ecg feature extraction techniques-a survey approach," *arXiv preprint arXiv:1005.0957*, 2010.

[16] R. Gupta, J. Bera, and M. Mitra, "Development of an embedded system and matlab-based gui for online acquisition and analysis of ecg signal," *Measurement*, vol. 43, no. 9, pp. 1119–1126, 2010.

[17] J. Andreasson, M. Ekstrom, A. Fard, J. G. Castano, and T. Johnson, "Remote system for patient monitoring using bluetooth," in *Sensors, 2002. Proceedings of IEEE*, vol. 1. IEEE, 2002, pp. 304–307.

[18] M. Malik, F. Farahmand, P. Otto, N. Akhlaghi, T. Mohsenin, S. Sikdar, and H. Homayoun, "Architecture exploration for energy-efficient embedded vision applications: From general purpose processor to domain specific accelerator," in *VLSI (ISVLSI), 2016 IEEE Computer Society Annual Symposium on.* IEEE, 2016, pp. 559–564.

[19] H. Zhou and H. Hu, "Human motion tracking for rehabilitationa survey," *Biomedical Signal Processing and Control*, vol. 3, no. 1, pp. 1–18, 2008.

[20] P.-J. Bristeau, F. Callou, D. Vissiere, and N. Petit, "The navigation and control technology inside the ar. drone micro uav," *IFAC Proceedings Volumes*, vol. 44, no. 1, pp. 1477–1484, 2011.

[21] S. Fleck, F. Busch, and W. Straßer, "Adaptive probabilistic tracking embedded in smart cameras for distributed surveillance in a 3d model," *EURASIP Journal on Embedded Systems*, vol. 2007, no. 1, pp. 1–17, 2006.

[22] L. M. Russo, E. C. Pedrino, E. Kato, and V. O. Roda, "Image convolution processing: A gpu versus fpga comparison," in *Programmable Logic (SPL), 2012 VIII Southern Conference on.* IEEE, 2012, pp. 1–6.

[23] S. Asano, T. Maruyama, and Y. Yamaguchi, "Performance comparison of fpga, gpu and cpu in image processing," in *2009 international conference on field programmable logic and applications.* IEEE, 2009, pp. 126–131.

[24] L. H. Crockett, R. A. Elliot, M. A. Enderwitz, and R. W. Stewart, *The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc.* Strathclyde Academic Media, 2014.

[25] XILINX, "Axi reference guide." [Online]. Available: https://www.xilinx.com/support/documentation/ip-documentation/ug761-axi-reference-guide.pdf

[26] R. Szeliski, *Computer vision: algorithms and applications.* Springer Science & Business Media, 2010.

[27] E. R. Dougherty, R. A. Lotufo, and T. I. S. for Optical Engineering SPIE, *Hands-on morphological image processing.* SPIE Optical Engineering Press Washington, 2003, vol. 71.

[28] B. Gerdle, S. Karlsson, S. Day, and M. Djupsjöbacka, "Acquisition, processing and analysis of the surface electromyogram," in *Modern techniques in neuroscience research.* Springer, 1999, pp. 705–755.

[29] U. Windhorst and H. Johansson, *Modern techniques in neuroscience research.* Springer Science & Business Media, 2012.

[30] "Signagel." [Online]. Available: http://www.parkerlabs.com/signagel.asp

[31] R. Merletti and M. Migliorini, "Surface emg electrode noise and contact impedance," in *Proceedings of the third general SENIAM workshop*, 1998.

[32] S. Day, "Important factors in surface emg measurement," *Bortec Biomedical Ltd publishers*, pp. 1–17, 2002.

[33] A. Industries, "Emg sensor." [Online]. Available: https://www.adafruit.com/

[34] C. J. De Luca, "Surface electromyography: Detection and recording," *DelSys Incorporated*, vol. 10, p. 2011, 2002.

[35] M. Z. Jamal, *Signal acquisition using surface EMG and circuit design considerations for robotic prosthesis.* INTECH Open Access Publisher, 2012.

[36] R. F. Coughlin and F. F. Driscoll, *Operational amplifiers and linear integrated circuits.* Prentice-Hall, Inc., 1987.

[37] G. De Luca, "Fundamental concepts in emg signal acquisition," *Copyright Delsys Inc*, 2003.

[38] J. Karki, "Active low-pass filter design," *Texas Instruments Application Report*, 2000.

[39] ALDEC, "High performance embedded development." [Online]. Available: https://www.aldec.com/en/products/embedded/tysom

[40] XILINX, "Xilinx analog to digital converter." [Online]. Available: https://www.xilinx.com/support/documentation/user-guides/ug480-7Series-XADC.pdf

[41] X. INC, "Axi dma ip." [Online]. Available: https://www.xilinx.com/support/documentation/ip-documentation/pg021-axi-dma.pdf

[42] I. RC Electronics, "Watt meter." [Online]. Available: http://www.rc-cars-planes.com/docs/wu100v2-user-manual.pdf

[43] I. P3 international, "Watt meter." [Online]. Available: http://www.p3international.com/products/p4400.html

Curriculum Vitae

Graduate College
University of Nevada, Las Vegas

Farhad Fallahlalehzari

Degrees:

Bachelor of Electrical and Electronics Engineering 2013
Islam Azad University, Karaj branch, Iran

Master of Electrical and Computer Engineering 2016
University of Nevada, Las Vegas

Thesis Title: EMG-based patient monitoring system using Zynq SoC device

Thesis Examination Committee:

Chair, Dr. Sarah Harris, Ph.D.
Committee Member, Dr. Shahram Latifi, Ph.D.
Committee Member, Dr. Venkatesan Muthukumar, Ph.D.
Graduate Faculty Representative, Dr. Stephen Benning, Ph.D.