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Kayla Cerminara

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TOWARDS HIGHLY SENSITIVE CAPACITANCE MEASUREMENTS OF A QUANTUM ANOMALOUS HALL PHASE IN VAN DER WAAL HETEROSTRUCTURES

By

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Bachelor of Science – Physics University of Nevada, Las Vegas 2020

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Abstract

One of the pioneering achievements in condensed matter physics of the 20th century is the observation of the quantum Hall effect (QHE) in which the Hall resistance in a two-dimensional (2D) sample takes on quantized values in the presence of a strong perpendicular magnetic field. The precise quantization of the hall resistance to one part in a billion has provided a practical, worldwide resistance standard. A long-standing goal has been to realize a similar state of matter but without the need of a strong quantizing magnetic field. The quantum anomalous Hall effect $(QAHE)$ is such a state that is predicted to exist in 2D materials with intrinsic magnetism and strong spin orbit coupling. Very few materials have these inherent properties, but new materials can be synthetically engineered by stacking and combining 2D layers into heterostructures with desired characteristics. In this thesis, we work toward combining graphene and few-layer graphene with materials that exhibit strong spin orbit coupling (molybdenum disulfide) with the goal of realizing a robust QAHE. To ascertain the presence of a zero-field gap in the electronic spectrum of the material, a benchmark of the QAHE, we implement a highly sensitive capacitance measurement technique. We present theoretical background on the quantum Hall effects and capacitance measurements to begin. We then present fabrication and measurements of four devices, two incorporating single layer graphene and two with bilayer graphene. Our work opens the door to prospective devices with utility in spintronics and topological quantum computing.

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Chapter 1

Introduction

The quantum anomalous Hall effect $(QAHE)$ is a robust, topologically protected phase of matter that has great potential in the fields of electronics, spintronics, and quantum computing $[6]$ $[7]$ $[8]$ $[9]$. In contrast with the well known quantum Hall effect $[10]$, the QAHE presents quantized resistances without the need of a high magnetic field, an impractical requirement for the above mentioned applications. In order for a material to exhibit the QAHE, it needs to have intrinsic magnetism and a significant spin orbit coupling (SOC) energy[11, 12, 13, 14]. Very few two-dimensional materials possess these attributes and the QAHE was first observed in a very complex system $(Cr_{0.15}(Bi_{0.1}Sb_{0.9})_{1.85}Te_3)$ grown by molecular beam epitaxy[15]. It would be advantageous to discover a more readily available, abundant material with these attractive properties.

Graphene, a single layer of graphite, has been a material of great interest due to its structural strength and its ability to allow electrons to easily flow through it (high mobility) [16]. Unfortunately, in graphene the SOC strength is very small and results in a minuscule electronic gap of $42 \mu\text{eV}$ [17] and it is also not intrinsically magnetic. This means graphene is not predicted to possess a QAHE on its own. Fortunately, it is possible to combine graphene with other materials by forming van der Waals heterostructures [18]. In these heterostructures, the adjoining materials can lend their properties to graphene

1

Figure 1.1: Theoretical calculations of the band structure of the predicted QAHE in bilayer graphene. Figure adapted from [1]. (a) A schematic of a van der Waals heterostructure of bilayer graphene sandwiched between a layer of a ferromagnetic insulator and a spin orbit coupling material (top left). The rest of the images are plots of the band structure of the theoretically predicted valley-polarized quantum anomalous Hall effect where the red (blue) band indicates the up (down) spins. (b) The band structure of a finite-sized 25 nm wide nanoribbon of the heterostructure shown in (a). The red bands represent the topological edge states and the gray shaded area is where the Hall resistance is predicted to be quantized at h/e^2 .

through proximity effects $[19, 20]$. It has been predicted that a QAHE can exist in bilayer graphene (two layers of graphene) if it is sandwiched between a ferromagnetic insulator (FMI) and a strong SOC semiconductor[1]. In figure 1.1 the predicted theoretical band structure is shown for the heterostructure. A model of the heterostructure is shown in figure 1.1(a) along with the conduction and valence bands of the band structure. Magnetism from the FMI splits the valence band degeneracy and SOC from the semiconductor splits the conduction band degeneracy (top right panel of figure 1.1(a)). By tuning the interlayer potential, *U*, with a perpendicular electrical field (provided by electrostatic gates), the bands with opposite spin can be made to overlap (bottom left panel of figure $1.1(a)$). With the addition of Rashba SOC, these bands hybridize and result in an inverted gap (bottom right panel of figure 1.1(a)). In a finite sized system (with edges) theoretical calculations predict edge states, the red bands in figure 1.1(b), that result in a quantized Hall resistance, a QAHE.

To determine the presence of the predicted hybridized gap, we employ sensitive capacitance measurements in this work. Capacitance measurements give information about a material's electronic structure through the thermodynamic density of states, *dn/dµ*, where *n* is the charge density and μ is the chemical potential [21, 22, 23]. This is helpful in the study of two dimensional materials including being able to easily and clearly detect electronic energy gaps, such as the one predicted for the QAHE in bilayer graphene. With the set up presented in this thesis, the capacitance measurements can probe individual layers of the van der Waals heterostructures.

This thesis will go over the properties of the quantum Hall effect that is seen in graphene, but incorporated with a SOC material, molybdenum disulfide, by using highly sensitive capacitance measurements. Chapter 2 will discuss the theory of Hall effect and its analogues, quantum capacitance and the density of states, and the various materials that are used. The process that is used to fabricate devices for the capacitance measurements will be found in Chapter 3. Then, in Chapter 4 the measurement techniques are outlined, including which instrumentation is used. The results are detailed in Chapter 5. Lastly, possible improvements and plans for future research are discussed in Chapter 6.

Chapter 2

Theoretical Background

This chapter reviews the theoretical background required to understand the experimental procedures and measurements performed, beginning with an overview of the Hall effect and its quantum analogues. It then goes on to describe classical and quantum capacitance and the differences between them. Lastly, it will cover the theoretical band structures for the materials used in these experiments.

2.1 The Hall Effects

2.1.1 Hall Effect

In a sheet of metal or semiconductor placed in a perpendicular magnetic field, one can apply a current and find there is a voltage difference across the perpendicular axis. Figure 2.1 shows a schematic model of the effect that occurs when a magnetic field, \bf{B} , is applied to the sheet of metal in the z-direction. If a current is applied to the metal along the y-direction, a voltage manifests in the x-direction. This phenomenon was discovered in 1879 by Edwin Hall $[24]$ and is aptly named the Hall effect. The Lorentz force acts on a charge carrier due to electric and/or magnetic fields, and it is responsible for deflecting the trajectory of charge carriers away from the y-direction[25]. The magnetic component can

Figure 2.1: The Hall effect occurs when a voltage is measured in the x-direction while a current is applied in the y-direction. This happens under the condition that there is an applied magnetic field in the z-direction.

be written as:

$$
\mathbf{F} = q\mathbf{v} \times \mathbf{B} \tag{2.1}
$$

where q is a charge moving at velocity **v** in the positive y-direction and **B** is the magnetic field acting on those charges. This causes the negative and positive charge carriers to accumulate on opposite sides of the material, producing an electric field in the negative (positive) x-direction for positive (negative) *q*. The electric force from this built-in field will eventually even out the magnetic force giving:

$$
q\mathbf{E} = q\mathbf{v} \times \mathbf{B},\tag{2.2}
$$

where E is the electric field due to the build up of charge in the x-direction. The trajectory of electrons experiencing the Lorentz force can be visualized in Figure 2.2a. Continuing, we can use the equation for current density, $\mathbf{J} = ne\mathbf{v}$, to give us:

Figure 2.2: The Hall effect and 3 of its analogues. (a) The Hall effect: the Lorenz force acting on the electrons in the presence of a magnetic field going into the page. (b) The Quantum Hall effect: The electrons undergo skipping orbits at the boundaries and the other states are localized in cyclotron orbits within the middle. (c) Anomalous Hall effect: The material acts the same as the hall effect, except without an applied magnetic field. (d) Quantum Anomalous Hall effect: The quantum Hall effect without the presence of an external magnetic field.

$$
E_x = -\frac{1}{ne} B_z J_y \tag{2.3}
$$

which allows us to arrive at the well-known Hall coefficient:

$$
R_H = \frac{E_x}{B_z J_y} = -\frac{1}{ne}
$$
\n
$$
\tag{2.4}
$$

where *n* is the number of electrons and *e* is the charge of the electrons.

2.1.2 Quantum Hall Effect

In 1980, it was discovered that if the measurements for the Hall effect were tested under helium temperatures $(4K)$ in a silicon field effect transistor subjected to a magnetic field of 15 T[10], the values of the Hall conductance became quantized at values of e^2/h and the longitudinal resistance dropped to zero. Figure 2.2(b) shows a model representation of the electronic states in a device exhibiting the quantum Hall effect (QHE). Here, skipping orbits at the edges of the sample result in dissipationless edge states and closed cyclotron orbits in the bulk of the sample produce insulating behavior. This picture is representative of the situation when the Fermi energy of the material lies between two Landau levels, whose energies are quantized to

$$
E_n = \left(n + \frac{1}{2}\right) \hbar \omega_c \tag{2.5}
$$

with *n* being an integer and ω_c is the frequency from the cyclotron orbit.

2.1.3 Anomalous Hall Effect

In ferromagnetic materials, it was realized that the Hall voltage was 10 times larger than in a nonmagnetic conductor. This discovery by Edwin Hall in 1881 was later dubbed the anomalous Hall effect (AHE). It has the same electrical response as the Hall effect, except without the presence of an external magnetic field. The Hall resistance for the magnetic material has two components: one that is proportional to the applied magnetic field and one that is proportional to the magnetization [26]. The latter is the anomalous contribution. The Hall resistance can then be written as:

$$
R_{xy} = r_0 H + r_\alpha M,\tag{2.6}
$$

where *M* is the magnetization of the sample, *H* is the applied magnetic field, and r_0 and r_α relate to the strength of the resistivities. Whereas the Hall resistivity r_0 depends on carrier

density, the anomolous resistivity r_α depends on a variety of material specific parameters[27]. Since the material itself is magnetic, it intrinsically breaks time reversal symmetry, a necessary ingredient for the Hall effect. Other factors that are responsible for this effect include spin orbit coupling and disorder effects. Panel c of figure 2.2 shows a visualization of the anomalous Hall effect.

2.1.4 Quantum Anomalous Hall Effect

It is logical then to wonder if the anomalous Hall effect can be quantized in the same sense as Hall effect. It has been shown that there is a quantum anomalous Hall (QAH) effect when time reversal symmetry is broken[12]. This requires the material to be a ferromagnetic semiconductor. The material has edge states with theoretically dissipationless currents called chiral edge channels. A QAH insulator is synonymous with a Chern insulator, meaning that it is a 2-dimensional insulator that has broken time-reversal symmetry. The chiral edge states are a characteristic of Chern insulators and are given by the Chern number.

2.2 Capacitance

To get an elementary idea of capacitors and measurements of capacitance, it is easiest to start with parallel plate capacitors. By connecting these plates to a battery and applying a potential difference, V , equal but opposite charge, q , will build on each of the plates. The charge and applied voltage are related in the following way:

$$
q \equiv CV \tag{2.7}
$$

where C is the capacitance. It is determined by the geometry of the plates of the capacitor and the dielectric that separates them $(C = A\epsilon/d)$.

Capacitance measurements can be performed in different ways. A simple meter can

Figure 2.3: (a) Example of a device used for capacitance measurements. Labeled are the source and the drain to the device, the material being probed or the channel, an insulating material, and a gate voltage applied to the bottom. (b-c) Plots of the density of states of a two band semiconductor for different gate voltages. The red line, μ , indicates the electrostatic chemical potential. (b) The density of states with no gate voltage. (c) When a negative voltage is applied to the device. The conduction band will move to be in line with μ . (d) When Fermi level is moved inside the the conduction band, the material becomes conducting.

measure capacitance by sending a known current through the device under testing (DUT) and measuring the rate at which the voltage rises. A fast rate of change in the voltage correlates to a smaller capacitance. This can be seen by rearranging equation 2.7 to $C = q/V$. The next method of measuring a capacitor is to pass a high frequency alternating current through the DUT and measure the voltage change across it. This is similar to the first method, but measured over several cycles of charging and discharging. The last and most precise way is to test capacitance by using a capacitance bridge. In this method, the DUT is placed in a circuit with a known capacitor. The capacitors are each paired with a resistor and the signal across them is changed until the circuit is balanced. The unknown capacitance can then be determined.

A majority of semiconductor devices are layered with a dielectric to isolate the gates from the channel. The capacitance of these devices is then the sum of the geometric capacitance from the dielectric and the quantum capacitance from adding carriers in the band structure of the semiconductor[21]. For devices with large density of states (DOS), the capacitance is just that of the geometric capacitance. On the other hand in low dimensional system, the effects of quantum capacitance outweigh that of the geometric capacitance because of the low DOS. Quantum capacitance is proportional to the density of states and can show us more subtle information about the system, like the band structure.

To show how the quantum capacitance is related to the density of states, we introduce the quantum capacitance of a simple two band semiconductor transistor (figure 2.3). Figure 2.3(a) shows a model of a device made with a semiconducting channel material. Figure 2.3(b-d) shows plots of the density of states for this semiconductor. The red line, μ , is the electrochemical potential. This is the level up to which the states are filled. When adding a negative gate voltage to the device shown in figure 2.3(a), the energy levels will float up, so that the electrostatic potential is right at the conduction band. To find the number of electrons, we can use the following equation [28]:

$$
N = \int_{-\infty}^{\infty} dED(E - U) f_0(E), \qquad (2.8)
$$

where $D(E)$ is how many electronic states there are at energy level *E* and f_0 is the fraction that are filled. With a transformation of variables, we arrive at the more useful equation:

$$
N = \int_{-\infty}^{\infty} dED(E) f_0(E+U). \tag{2.9}
$$

When the electrostatic potential is inside the conduction band, figure 2.3(b), we can find the quantum capacitance of the device by calculating how the number of charged particles, *N*, changes with a small change in the channel potential, *U*. We can start by taking the derivative of equation 2.9 with respect to the chemical potential.

$$
\frac{dN}{dU} = \int_{-\infty}^{\infty} dED(E) \frac{\partial f_0(E+U)}{\partial E}.
$$
\n(2.10)

This quantity will be negative because of the Fermi function and it will give the average density of states, D_0 .

$$
\frac{dN}{dU} \equiv -D_0.\tag{2.11}
$$

Here, $-D_0$ is the average density of states in the energy range of interest. If we go on to find the change in the charge due to the change in the potential, we find that it is equal to the quantum capacitance,

$$
\frac{d(qN)}{d(\frac{U}{-q})} = q^2 D_0 \equiv C_Q,\tag{2.12}
$$

or

$$
\frac{dN}{dU} = -D_0 \equiv \frac{-C_Q}{q^2}.\tag{2.13}
$$

Figure 2.4: Graphene crystal structure and energy band structure. Figure adapted from Castro Neto et al. [2]. (a) The crystal structure for monolayer graphene. It is a honeycomb lattice made up of carbon atoms. (b) The crystal structure for multiple layers of graphite is monolayer graphene stacked on top of itself. (c) Graphene's band structure with hopping values of $t = 2.7eV$ and $t' = -0.2t$. The inset shows a zoomed in picture of one of the Dirac cones.

This shows us that by measuring small changes of the quantum capacitance, we get a picture of the density of states of the material.

2.3 Material Theory

We now move to a more general discussion of the theoretical properties of the materials of interest in our work. We start with graphene, a single layer of graphite, continue with molybdenum disulfide $(MoS₂)$, a transition metal dichalcogenide, and finish with boron nitride (BN).

2.3.1 Graphene

Graphene has been a material of interest since its discovery in the condensed matter field[29]. Graphene is a 2-dimensional system notable for its high electron mobility, meaning that the electrons can flow easily through the material, making quantum effects easily distinguishable. Capacitance measurements are ideal for graphene because of the ability to easily tune the electrical properties with an electrostatic gate. In 2004, it was

found that graphite can be exfoliated down to a single layer of atoms by using the scotch tape method [16]. There are 3 thicknesses of few-layer graphene that are of interest to us: monolayer, bilayer, and trilayer.

For monolayer graphene, the electronic band structure can be calculated from a tight-binding Hamiltonian [2]:

$$
H = -t \sum_{\langle i,j \rangle, \sigma} (a_{\sigma,i}^{\dagger} b_{\sigma,j} + H.c.) - t' \sum_{\langle i,j \rangle, \sigma} (a_{\sigma,i}^{\dagger} a_{\sigma,j} + b_{\sigma,i}^{\dagger} b_{\sigma,j} + H.c.), \tag{2.14}
$$

where $a_{i,\sigma}$ and $a_{\sigma,i}^{\dagger}$ are the annihilation and creation operators with spin, $\sigma = \uparrow, \downarrow$. This Hamiltonian will produce the following energy bands [30]:

$$
E_{\pm} = \pm t\sqrt{3 + f(\mathbf{k})} - t'f(\mathbf{k}),\tag{2.15}
$$

where

$$
f(\mathbf{k}) = 2\cos(\sqrt{3}k_y a) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right). \tag{2.16}
$$

In equation 2.15, the plus sign represents the upper band and the minus sign represents the lower band. If $t' = 0$, we can see that it is symmetric around zero energy, but with a finite t' the bands become asymmetric because of the electron-hole symmetry being broken. Figure 2.4(c) shows the energy spectrum with finite t and t' and the inset of the figure shows one of the Dirac cones.

To observe quantum anomalous hall effect, a material needs to have intrinsic magnetism and a strong spin orbit energy. Unfortunately graphene has neither of these properties intrinsically and so we look to other materials, such as $MoS₂$ with strong spin orbit coupling.

Figure 2.5: The theoetical band structure of $MoS₂$, calculated from first priciples. This figure is adapted from [3]. (a) The *d* orbital contribution. (b) The *p* orbital contribution. (c) The *s* orbital contribution.

2.3.2 Molybdenum Disulfide

Recently, transition metal dichalcogenides (TMDCs) have been studied for use in electronics and opto-electronics [31]. Molybdenum disulfide $(MoS₂)$ is one of these TMDCs. A monolayer of $MoS₂$ consists of a single layer of molybdenum that is sandwiched between two sulfur layers. Graphene is similar to $MoS₂$ in the sense that the conduction and valence bands are located at the first Brillouin zone at the K and \overline{K} points [3]. MoS₂ differs from graphene in several ways. It is a semiconductor, whereas graphene has no band gap. The second main difference is that MoS_2 has a strong spin-orbit coupling from its heavy metal atoms [32].

Figure 2.5 shows the calculated band structure for $MoS₂$ from first principles and the separate contributions from the *d*, *p*, and *s* orbitals [3]. It can be seen that $MoS₂$ is a semiconducting material with a band gap of approximately 1.8 eV.

Figure 2.6: The crystal structure[4] and the band structure[5] of hBN. (a) Multi-layer BN is similar to graphite in that the bulk structure is composed of monolayers stacked on top of one another. (b) Monolayer BN has the same hexagonal or honeycomb structure as graphene. (c) The LDA (local density approximation) band structure of bulk hBN. (d) The GW (Coulounb-Green's function approximation) band structure of bulk hBN.

2.3.3 Hexagonal Boron Nitride

Hexagonal boron nitride (hBN) has an atomically smooth surface and it has interatomic spacing close to that of graphene, but has a large band gap in comparison to graphene [4]. This makes it an ideal candidate as an insulating layer in our devices. hBN has a honeycomb lattice and has alternating boron and nitrogen atoms. The crystal structure of hBN can be seen in figure 2.6(a-b).

Figure 2.6(c-d) show the band structure of bulk hBN. The local denisity approximation (LDA), shows that hBN has a band gap of 3.9 eV, making it a wide-band gap semiconductor^[5] but effectively insulating in our experiments.

Chapter 3

Fabrication Processes for Capacitance Devices

This chapter discusses the different materials and techniques used to fabricate the devices used to make capacitance measurements. These materials include graphite, hexagonal boron nitride (hBN), and molybdenum disulfide $(MoS₂)$. The chapter begins with stack design, the process we use to design our heterostructure stacks before creation. This section includes descriptions of the exfoliation of the materials and our stacking technique used to combine the individual materials into a complete stack. The chapter continues with photolithography, a process that allows us to create micron-sized patterns on the surface of our heterostructures for the purpose of etching and to create electrical contacts. The chapter concludes with a discussion of our etching process that allows us to etch away unwanted portions of the heterostructures.

3.1 Stack Design

Summarizing the stack design, the materials we exfoliate are used to design the devices. The stacks are designed to have a relatively large, $20 \mu m$ by $20 \mu m$, overlap area with limited amount of extra overlap of the materials. It is necessary to only have the

Figure 3.1: Overview of the stack design and etching. (a) A model of a representative heterostructure. There are two graphite gates on the top and the bottom of the stack. There is then an insulating layer of material next to the gates, with the graphene and Mo_2 in the middle. (b) An optical image of a stack before the etching process. (c) An optical image of the same stack after the excess material has been etched away.

materials overlap in the same area. Extra overlap of the graphite gates without graphene in between, for instance, will result in a capacitance signal derived only from the gates themselves and not the material of interest between the gates. Figure 3.1(a) shows a model of a heterostructure stack and the order, starting from the top layer, of the stacks. The outside is sandwiched with graphite, while there is a layer of BN insulating the graphene and $MoS₂$ in the middle. The graphite layer is first picked up with a large BN flake (not shown). Subsequent flakes are picked up in the same order, from top to bottom, until the entire stack is complete. Figures $3.1(b)$ and $3.1(c)$ show optical images of a completed stack that was used for measurements described in later chapters. The middle panel shows the stack before the excess overlap was etched away and right panel shows the stack after the etching process.

3.1.1 Exfoliation

After we have a design for which materials we would like to use and how we will stack them, we can start looking for the materials that we will use. The materials are exfoliated

onto a 500 μ m thick silicon (Si) chip with a 300 nm layer of silicon dioxide (SiO₂). The chips are made by dicing a 4 inch wafer into 10 mm squares with a diamond tipped scribe. The material is exfoliated by using the scotch tape method [16, 33]. The basic process for exfoliating the materials is the same, but some small variations in the process are utilized to increase the yield of high quality flakes. When exfoliating BN, a few small bulk pieces are placed on the tape. When exfoliating other material, the tape is pressed on small millimeter sized pieces. The tape is then adhered to itself and pulled apart until there is what looks to be an even layer of material on the tape. We call this the parent tape. Another piece of tape is then taken and adhered to the parent tape and pulled off. This is the daughter tape. The daughter tape is then placed on to the $Si/SiO₂$ chips. When exfoliating BN, the tape is pressed down firmly with a finger tip for approximately 10 seconds before being pulled off slowly. When exfoliating graphite and $MoS₂$, the tape is flattened with the backside of a razor blade and then slowly pulled off. The different methods used for these materials are due to the structures of the materials. Graphite and $MoS₂$ have a lower cleavage energy and more malleable character when compared to BN, leaving thinner flakes of material. The chips with the material are then scanned with an optical microscope under white light illumination. Images are taken of flakes of material for potential stacks. Figure 3.2 shows several optical images of flakes used to make the first few layers of the model heterostructure in panel d. Flakes are chosen based on their thickness and surface area. The thickness of the flakes can be determined by using image contrast comparisons[34, 35, 36]. To perform a contrast comparison, the image is first loaded into imaging software (Gwyddion). Using the software, a contrast profile can be taken across the flake, showing the contrast difference between the background $(Si/SiO₂)$ and the flake itself. The contrast difference can be compared with values reported in literature to determine the flakes thickness[34]. This method is reliable for mono and few layer flakes but becomes unreliable for several layers. The general color of the flakes can also be used as a guide to the approximate thickness. For instance, the graphite flake in

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Figure 3.2: Optical microscopy images of various flakes of materials that have been exfoliated using the Scotch tape method. These include: (a) Flake of BN that is used as the first pick up layer due to the large surface area. BN is also used as an insulating layer in between stack. (b) Flake of graphite that was used as a top gate. The graphite that is used for gates is typically $>$ 5 layers. (c) Flake of bilayer graphene (d) Flake of $MoS₂$. MoS₂ is used with graphene due to its larger spin orbit coupling energy.

panel b of Figure 3.2 is purple and can be approximated as having a thickness of 5 - 10 layers. This thickness is suitable for a top or bottom gate.

3.1.2 Stacking

Once we have the stack designed and the different flakes that we want to use ready, we can begin the stacking process. Traditionally, this method was done using a polypropylene carbonate (PPC) film to pick up the different layers of the stack $[37, 38]$. Recently, our lab has developed a stacking process using common household nail polish[39]. Not only is this process more cost effective, but it is less complicated and leaves us with high quality stacks.

To stack these materials using nail polish we start with a glass microscope slide. A cylindrical piece of polydimethylsiloxane (PDMS) is stamped out of a thick film (5 mm thick) using a biopsy punch that is about 3 mm in diameter and placed towards one end of the glass slide. A piece of clear Scotch tape is placed over the PDMS in order to create a raised area that we refer to as a hemisphere. We then place a drop of Revlon clear nail polish on the center of the hemisphere using a toothpick. The glass slide is then placed on

a hot plate at 90C for approximately 1 minute to cure and harden the nail polish.

This glass slide is then loaded into a micromanipulator with the hemisphere side facing down. The micromanipulator is positioned over a stage under an optical microscope. A model representation of this can be seen in figure 3.3(a). A $Si/SiSO₂$ chip with a flake of interest on it is placed on the center of the stage. The micromanipulator is then used to lower the glass slide over the "chosen" flake until the nail polish touches down on the $Si/SiSO₂$ chip. Figure 3.3(a-c) shows this process for the first BN pick up. After the slide pins part of the BN with the nail polish, it is slightly lowered until the nail polish envelops the whole flake of BN. The slide then can be brought back up quickly, with a popping motion. The adhesion force from the nail polish is enough to pick up the first BN and it is strong enough to undergo the abrupt motion. For subsequent flakes, van der Waals forces between the other materials are used to pick them up. The process to find the flake is repeated (figure $3.3(d)$). The difference comes in when needing to pick up the flake. The stage has a heater that is initially set at 40° C. Once the flake is pinned on a corner with the BN on the nail polish, the heater is slowly raised 2° C at a time (figure 3.3(e)). The contact between the nail polish and the surface will slowly grow and envelope the flake. The temperature increase is stopped once the flake is fully covered by the nail polish. This usually happens around 50° C-60 $^{\circ}$ C. The temperature is then held there for about 1 minute until it is reset to its starting point of 40° C. When the temperature is reset, it slowly comes down, causing the contact to shrink and pull up the flake as seen in figure 3.3(f). This process is repeated until all flakes are stacked on the nail polish hemisphere.

The next step in this processes is to transfer the stack to a chip made of either quartz or undoped silicon. These materials are used because they are insulators and will not contribute to stray capacitance during the measurements. The chips have an outer ring of electrode pads prepatterened out of gold. The chip is placed on the stage. The glass slide is positioned using the micromanipulator in order to transfer the stack to the center of the chip. The heat of the stage is set to 40° C. The slide is slowly lowered down onto the chip

until part of the stack is pinned in between the nail polish and the chip. The heat is increased by 20° C and held at the that temperature for about 5 minutes. The nail polish will start to spread out and cover the stack. The z-axis control on the micromanipulator is used in order to keep the whole chip from laminating. This process is repeated again, so that the temperature is at 80° C. From here, the stack can be squeezed.

The squeezing process will help push the bubbles containing water and adsorbates out from in between layers, creating a better contact. To squeeze the stack, the z-axis of the micromanipulator is used to pull up the stack and push it back down, always keeping one part of the stack pinned. After the stack is squeezed, the temperature is brought up again by 20° C at a time. After each temperature raise, the temperature is held for about 5 minutes. This process repeats until the temperature reaches 110° C, melting the nail polish completely. The temperature is held here while the z-axis is slowly brought up. The glass slide is pulled up until the nail polish detaches from the chip. The chip is placed in a bath of acetone for about 10 minutes or until all of the nail polish is removed. This chip is rinsed with IPA and dried carefully with a nitrogen gun.

3.2 Photolithography

After the stack has been transferred to the chip with the gold pre-electrode pattern, the stack then undergoes a photolithography process in order to create a mask to etch the stack and then later pattern electrodes to each layer. This process is performed at the UNLV Nanotechnology Center, a class 1000 cleanroom located in the Science and Engineering Building.

First we design a pattern for the etch mask in CAD software. The design of the mask for the stack is made to maximize device area while etching away any unwanted overlap of materials. The pattern of the mask is then loaded into the photolithography software.

For patterning the mask, two different recipes were tested. The monolayer recipe

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Figure 3.3: Overview of the stacking process that is used to fabricate the devices that we use for capacitance measurements. The first row of figures shows how the first piece of BN is picked up using adhesion forces from household nail polish. The second row of panels shows how later flakes are stacked using the van der Waals forces between the materials. The last row of images is how the stack is transferred to a substrate of choice. (a) At the top is the glass slide with the hemisphere, in blue, that is created by layering a piece of clear tape over a cylinder of PDMS. A drop of nail polish is then put on the top of the hemisphere. At the bottom shows a flake of BN that has been found on top of a $Si/SiO₂$ chip. (b) The glass slide is slowly lowered over top of the flake using the z-axis on the micromanipulator. The nail polish drop then pins a corner of a flake of material and is continuously brought down until the flake has been covered. (c) The slide is pulled up quickly, taking the flake of material with it. (d) The slide with the BN is positioned over the next flake of material. (e) The slide is slowly lowered pinning a corner of a flake of material with the BN. Heat is applied from the stage in increments of 2° C until the flake is covered by the BN and nail polish. This happens around 48° C. (f) The heat is then lowered back to 40° C and the z-axis is used to slowly bring up the picked up flake. The materials should now be stacked on top of each other. (g) To transfer the whole stack, the slide is positioned in reference to the electrode position on the chip that the stack will be transferred to.(e) The slide is lowered and a corner of the stack is pinned to the substrate. The heat is raised in increments of 20° C. The z-axis is used to keep the nail polish from laminating the while chip and keeping the nail polish to the area around the stack. The heat is stopped once it reaches 110° C. (f) The heat is held at 110° C while the z-axis is used to slowly pull up the glass slide.
consisted of only spinning photoresit on to the chip. This recipe was found to be best when depositing the 80 nm chromium (Cr)/gold (Au) electrodes. When depositing copper (100 nm), the excess copper would not cleanly lift off and leave the copper mask behind for etching. A bilayer recipe was developed to overcome this difficulty. This recipe involves spinning a layer of lift off resist (LOR) before spinning a layer of photoresist on to the sample. After the pattern has been exposed, the developer will dissolve the LOR slightly faster than it does the photoresist. This will leave an undercut under the photoresit layer, which helps with the removal of the excess copper.

To prepare the sample for photolithography with the bilayer recipe, the chip with the stack on it is placed on a spinner and held by a vacuum. First, LOR is dropped on the chip with a pipette and is let to sit for 1 minute to promote adhesion. Then the LOR is spun on the chip for 30 seconds at 2000 RPM. The chip with the LOR is transferred to a hot plate at 190C for 5 minutes. The chip is then returned to the spinner and photoresist is dropped onto the chip. The photoresist is then spun on the chip for 30 seconds at 4000 RPM. The chip is transferred to the hot plate at 95° C for 60 seconds. These spinning recipes result in a layer of LOR with a thickness of approximately 300 nm and a layer of photoresist with a thickness of about 1 micron.

The chip is placed on a stage of a Microlight 3D Smart Print. The Smart Print allows us to use lithography techniques with a digital mask pattern as opposed to a hard mask. This allows us to expose custom patterns onto any device without the need to first create a hard mask. This is very convenient when designing electrodes or masks for etching. The smallest resolution that we can achieve is $2 \mu m$. The exposure time and objective size is chosen depending on what material the chip is and how big the pattern is. For a quartz chip, slightly longer exposure times are used compared to a $Si/SiO₂$ chip. The difference in exposure times is due to the opacity of the material. The different exposure times can be seen in table 3.1 and 3.2. The 10x objective size is used to make the pattern for the etch mask. The pattern is lined up to the stack and exposed. The chip is placed in developer

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and lightly swirled for 60 seconds to remove the photoresist and LOR that was exposed with the Smart Print. The UV light from the Smart Print breaks the polymer bonds in the LOR and resist so that the developer can remove the material from the pattern areas.

Table 3.1: Exposure times when doing a monolayer photoresist mask

		Objective Substrate Exposure time [s]	
10x	Si/SiO ₂	0.8	
2.5x	Si/SiO ₂	$3.7 - 3.8$	
2.5x	Quartz	4.5	

Table 3.2: Exposure times when doing a bilayer LOR/photoresist mask

For an etch mask we use copper which is deposited to the chip surface using a benchtop sputter system. The thickness of the copper layer is approximately 100 nm. The chip is then placed in resist remover to lift off the unwanted copper. This will leave only the pattern with the copper layer and the unwanted parts of the stack exposed for etching. The etching process will be discussed in detail in the next section: 3.3.

After the etching process, the chips go through the photolithography process again to deposit and create electrical contacts to the stack layers. This time a single layer photoresist mask recipe is used. The single layer recipe works best for the Cr/Au electrode deposition without wasting excess lithography materials. Photoresist is spun on the chip for 30 seconds at 4000 RPM. The chip is placed on a hot plate at 95° C for 60 seconds. The chip is then placed on the Smart Print stage and aligned to expose an electrode pattern that connects the larger outer pads to the stack. The chip is then placed in developer and swirled for 60 seconds. Figure 3.4(a) shows an example of the chip after the electrode

pattern has been created. The brown areas in the image show the chip surface and the green areas show the resist. The heterostructure is located in the middle of the image. Three electrodes have been patterned for this stack. One for each of the gate electrodes and one to contact the middle layer of graphene and M_0S_2 . The stack is then placed in an electron beam deposition chamber. 10 nm of chromium is deposited and then an 80 nm layer of gold is deposited on top of the chromium. Figure 3.4(c) shows the stack after the electrodes have been deposited and the unwanted gold has been removed. Now, the brown regions are the substrate surface and the gold regions are the electrodes. Figure 3.4(d) shows a lower magnification image of the same stack showing the connections made to the larger prepatterned electrodes.

3.3 Etching

This is a critical step for the capacitance devices, and so we have devoted a separate section to this process which took several months to work out. Ideally when devices are fabricated, the materials are only overlapped in the same area. Unfortunately, it is unrealistic to line up the materials perfectly during the stacking procedure because all the flakes have different shapes. This causes the need to get rid of any unwanted overlap. After lithography and the copper mask has been deposited onto the stack, the stacks are etched in a plasma etcher. The stacks are etched by alternating gasses, O_2 and CHF_3 , depending on what layers need to be removed. Table 3.3 shows the different etching parameters that are used. Figure 3.5 shows a stack after several etching steps. The first image (a) shows the stack before any processing has been done on it and the second image (b) shows the stack after the copper mask has been sputtered on it. For the stack design that is shown in section 3.1, these formulas are alternated, starting with the hBN formula. Figure $3.5(c)$ shows the stack after this first etch. After each trial of etching, the stack is viewed under an optical microscope to see which layers are left and judge which formula to use (figure

Figure 3.4: Optical images of a device after the photolithography processing and after gold electrodes have been deposited. (a-b) A mask is applied to the device using photolithography techniques. This mask is a single layer of photoresist. The brown regions are the exposed substrate surface after development and the green regions show where the resist still resides. (c-d) Gold is deposited to the chip using an electron beam deposition. The resist mask is removed using acetone and the gold electrodes are left where the photoresist was exposed.

3.5(d-i)). Once all of the material is removed that is not under the copper mask, the mask itself can be removed using an ammonium persulfate solution as seen in figure 3.5(j).

Table 3.3: Etch times depending on which material is being removed. Both of the recipes use 100 W of power.

Material	$CHF_3 \,[\text{mL/min}]$ $O_2 \,[\text{mL/min}]$ Time $[s]$	
Gr and $MoS2$		

Figure 3.5: Optical images of a stack undergoing an etching process. (a) An optical image of the stack before the copper mask has been deposited. (b) The stack after the copper mask has been deposited, before etching has started. Images (c-i) are after different etching formulas for the different materials: (c) BN, (d) Gr, (e) BN, (f) Gr, (g) $MoS₂$, (h) BN, and (i) Gr. The last image (j) shows the stack after the copper mask has been removed.

Chapter 4

Instrumentation and Measurement

After the device has been patterned to electrodes, it is bonded to a capacitance bridge on a sample holder that will go into a cryostat (Quantum Design Physical Property Measurement System, PPMS). The capacitance bridge allows us to measure the small capacitance signals that are associated with our small micron-sized devices. Traditionally, capacitance bridges have been able to make measurements on devices that have a larger density of states (DOS). In the devices that we make, quantum capacitance outweighs the geometric capacitance due to their low DOS. With the setup that is described in this chapter, we are able to resolve attofarad (aF) quantum capacitance signals [40]. In this section, the setup for the capacitance bridge will be described, then the connections that are made from the capacitance bridge in the cryostat to the outside electronics will be reviewed, and lastly the actual measurement procedure will be discussed.

4.1 Instrumentation

4.1.1 Capacitance Bridge

The capacitance bridge setup will make highly sensitive capacitance measurements, on the order of attofarads (aF) at room temperature [40] [41] [42] [43]. We will also refer to it

Figure 4.1: Schematic of the electrical setup used to make the capacitance measurements. The red outlined portion represents the electronics and device that are located inside the cryostat. See the main text for further descriptions.

as a transistor mount due to the geometry of the transistor on the capacitance bridge.

A traditional capacitance bridge circuit will have two capacitors, one with a known capacitance and one with an unknown capacitance. It will also have two resistors, where one or both are adjustable. These are all connected to what can be called a bridge point. An AC supply is applied to the circuit until the bridge point is balanced at zero voltage.

The capacitance bridge is connected to the device under test (DUT) and put into the cryostat. In figure 4.1, the electrical schematic of the capacitance bridge with the sample can be seen outlined in red. The sample is a triple layer capacitor made of two electrostatic gates and one middle layer. The purple line in the center of the sample (top right) represents the graphene. There is a voltage that is applied to the graphene, signified by *Vsamp*. A voltage, *Vtop* is also applied to the top gate that has been added to an oscillating signal from the function generator. The function generator also applies a signal to the reference capacitor. This is in line with a voltage that goes through a 100 M Ω resistor and then runs to the gate of a Fujitsu FHX35X low noise high electron mobility transistor (HEMT). The HEMT is used as an impedance matching amplifier. It is attached to a printed circuit board (PCB) vertically with solder. The mounting of the HEMT is vertical so that the two dimensional electron gas of the transistor is parallel to the magnetic field. This setup with the sample will create a balance point, labeled in Figure 4.1 (top left). This point balances the geometric capacitance of the device and any unimportant parasitic capacitance. The HEMT is voltage biased with a 1 k Ω resistor for stable operation around the maximal gain of the amplifier.

4.1.2 Cryostat to Measurement Electronics

The capacitance bridge, along with the DUT, is bonded to a sample holder (PPMS puck) that is lowered into a Quantum Design Evercool II cryostat. The PPMS is a cryostat that can achieve low temperatures, 2 Kelvin, and high magnetic field with a superconducting magnet, up to 9 Tesla. The device is wire bonded to a puck that is

inserted into the cryostat and connected with the internal electronics that we are able to access from outside of the cryostat through a breakout box that was made in the lab.

Outside of the cryostat, we have the electronic set up that includes a digital-to-analog/analog-to-digital converter (DAC-ADC), SR-830 lock-in amplifier, and a function generator. The DAC-ADC can supply a voltage *±*10 V and read a voltage on a chosen channel. The breakout box is used to make connections to the device inside of the cryostat.

4.2 Capacitance Measurements

With this set up, we measure the penetration field capacitance of the device. The penetration capacitance is related to the electronic compressibility. This gives a clear picture of the electronic states of the material. The penetration field capacitance can be written as[20]:

$$
C_p = \frac{c^2}{2c + \frac{\partial n}{\partial \mu}}\tag{4.1}
$$

where *c* is the geometric capacitance, μ is the chemical potential, and $\frac{\partial n}{\partial \mu}$ is the thermodynamic density of states[23] or bulk compressibility. At the balance point, we sweep *Vsamp* and *Vtop* to measure the changes in the penetration field capacitance for different charge density (n) and field polarization (p) .

Chapter 5

Results

This chapter will go over the results that were obtained for this thesis. The capacitance was taken for each device by measuring the penetration capacitance (C_p) . The penetration capacitance is normalized by the reference capacitor (C_{ref}) in the capacitance bridge. These values are measured by applying a small AC excitation to the top gate of the device and then adjusting the excitation on the reference capacitor to balance the bridge (see also figure 4.1). Once the balance point is found, we sweep the top and sample DC voltages to change the charge density (n_0) and the layer polarization (p_0) . These are related through the following simple equations:

$$
\frac{n_0}{c} = v_t + v_b \tag{5.1}
$$

$$
\frac{p_0}{c} = v_t - v_b \tag{5.2}
$$

where v_t (v_b) is the top (bottom) gate voltage. The data we present will be the changes in the penetration field capacitance as a function of the charge density (number and type of charge carrier) and the layer polarization (the orientation and strength of the electric field that penetrates the stack). The penetration field capacitance will be relatively high (at the balance point) when the graphene layer is insulating and low when the graphene layer is more conducting.

The chapter will start by reviewing the data that was taken on devices with monolayer graphene and M_2 . Then, it will present the data from devices with bilayer graphene and $MoS₂$.

5.1 Monolayer Graphene on MoS_2

There are two monolayer devices that were tested. Both of these devices were fabricated with an $MoS₂$ flake below the graphene flake to investigate a spin orbit coupling proximity effect that has been reported in literature $[44, 45, 46, 47]$. It has been shown that when graphene is placed on top of a strong spin orbit coupling material, such as $MoS₂$, it will inherit some of this interaction through what is called a proximity effect. This proximity effect can lead to two types of induced spin orbit coupling, an ising spin orbit coupling and a Rashba spin orbit coupling. We aimed to investigate this proximity effect in our devices.

The first device presented is JMA002. Figure 5.1 shows an optical image of the device in panel a. This device was made with monolayer graphene that is in contact with the $MoS₂$. There is a piece of BN on each side of the graphene/ $MoS₂$ to insulate it from the graphite gates that are on the outside of the stack. The schematic of the stacking order can be seen in figure $5.1(b)$.

Capacitance measurements for JMA002 were first taken without an applied magnetic field at 2 K in a cryostat. Figure $5.1(c)$ is the 2D plot of these measurements. The measurements resemble earlier reports of capacitance measurements of monolayer graphene [23]. C_p is plotted as a function of p_0/c on the vertical axis and n_0/c on the horizontal axis. The reduction in the density of states of graphene around the Dirac point can be seen at $n_0/c \approx 0$ as the peak in the capacitance signal. There is also a weak peak in the form of a

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Figure 5.1: This figure shows data that was obtained from device JMA002. (a) An optical image of the device with patterned gold electrodes. (b) A digitally drawn schematic of the layers of JMA002. There is monolayer graphene in contact with $MoS₂$. These two materials are sandwiched on each side by BN and graphite gates. (c) 2D plot of the penetration capacitance (C_p) , scaled by the reference capacitor (C_{ref}) , plotted as a function of charge concentration (n_0/c) and polarization (p_0/c) taken at 2 K. (d) A line cut taken of plot in (c) at $p_0 = 7V$. The peak is due to the reduction in the DOS of the graphene flake. (e) 2D plot of C_p/C_{ref} as a function of n_0/c and p_0/c taken at 2 K and 9 T magnetic field. The plot shows the quantum hall gaps as vertical lines starting in the middle at 0 V and working outwards. (f) A line cut of plot of the data plotted in (e) taken at $p_0 = 5$ V. The filling factors can be seen as local maxima, starting at 0 V and working outwards.

diagonal line around $p_0/c = 0$ V. We do not know the precise origin of this weak peak, but it could come from another dislocated piece of graphene within the stack but with different gate coupling. Figure 5.1(d) shows a 1D plot where a line cut was taken at $p_0/c = 7$ V. The line has a peak at $n_0/c = 0$ V that comes from the graphene reduced DOS.

For the rest of the measurements that were taken, a magnetic field of 9 T was applied to the device. The 2D plot seen in figure 5.1(e) shows the integer quantum Hall gaps that arise[23]. They can be seen as peaks in the capacitance signal, with smaller peaks surrounding $n_0/c = 0$ V and with the largest peaks in capacitance at around $n_0/c = 2$ V, which corresponds to the 3 and -3 filling factors. Diagonal lines can be seen cutting through the signal that are picked up from the spurious graphene flake. A line cut of the 2D plot taken at $p_0/c = 5V$ is shown in figure 5.1(f) where the quantum Hall gaps are seen as the local maxima.

The second monolayer device is KC011. The optical image of the device can be seen in figure 5.2(a). The device has monolayer graphene with MoS_2 that has been sandwiched with BN and then graphite to use as the top and bottom gate (figure $5.2(b)$).

The data that was taken for KC011 at 2 K with no external magnetic field can be seen in figure 5.2(c). This is a plot of the capacitance as a function of the charge concentration and the polarization. The bright orange line down the center of the 2D plot is due to the decrease in the DOS of graphene near the Dirac point. A diagonal dip (light blue) can also be seen in this plot. We are uncertain of the origin of this capacitance signal but it may be associated with spurious quantum capacitance changes in the thin gate electrodes. In figure $5.2(d)$, a line cut was taken of the 2D plot at a polarization of 4 V. The graphene Dirac point can be seen as the peak at $n_0/c = 0$ V.

Measurements were then taken with an applied magnetic field of 9 T. The results of these measurements can be seen in figure $5.4(e$ and f). The 2D plot shows the different integer quantum Hall gaps that occur due to the quantizing magnetic field. These can be seen as peaks in the capacitance values, starting at $n_0/c = 0$ V as the zeroth filling factor.

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Figure 5.2: This figure shows the data that was obtained for device KC011. (a) An optical image of the device. (b) A digitally drawn schematic of the layers of KC011. There is monolayer graphene that is in contact with $MoS₂$. These two materials are sandwiched on each side by BN and graphite gates. (c) 2D plot of the penetration capacitance (C_p) , scaled by the reference capacitor (C_{ref}) , plotted as a function of charge concentration (n_0/c) and polarization (p_0/c) taken at 2 K. (d) A line cut of the data plotted in (c) at a polarization of 4 V. (e) 2D plot of the penetration capacitance (C_p) , scaled by the reference capacitor (C_{ref}) , plotted as a function of charge concentration (n_0/c) and polarization (p_0/c) taken at 2 K and 9 T. The quantum hall gaps show up in the plot as vertical lines, starting with 0 at $n_0/c = 0$ V and working outwards. (f) A line cut taken from plot (e) at $p_0/c = 5$ V. The quantum hall gaps can be seen as local maxima start in the middle at $n_0/c = 0$ V and working outwards.

The filling factors then work their way outwards from the center taking values 1, -1, 2, -2, etc. The 1D plot is a line cut taken at $p_0/c = 5$ V. The local maxima where the capacitance peaks are the various filling factors for the quantum hall gaps.

Summarizing our results on the monolayer graphene devices, we did not see a clear indication of the $MoS₂$ flake or its possible effect on the graphene capacitance signal. In order to further investigate these types of devices, we aim to perform weak antilocalization measurements which will allow us to extract charge scattering rates associated with spin orbit coupling [44].

5.2 Bilayer Graphene on MoS_2

Two bilayer devices were tested for this thesis. Both of these devices were fabricated with an MoS_2 flake incorporated in the stack.

Measurements for the device KC004 were first taken at room temperature. The optical image and the stacking schematic are shown in figures 5.3(a and b). In figure 5.3(c) the conduction band edge of the $MoS₂$ can be seen clearly. This edge delineates the insulating gap (red portion) from the conducting band (blue portion).

The device was then cooled down to 2 K, without an applied magnetic field (figure 5.4(a-b)). The 1D line cut of the plot was taken at $n_0/c = 5$ V, which shows a linear relationship between the capacitance and the polarization. This is because the transistor mount temperature was not stable, causing the amplifier to change over time producing a slowly varying capacitance signal. To remedy this, the background was subtracted by taking a line cut at $n_0/c = -5$ V and then subtracting it from each line of the 2D plot. This gives the plots from figure 5.4(c-d). The expected relationship is shown between the conduction band and band gap of the $MoS₂$, with the conduction band shown in blue and the band gap in red. There is a sharp peak in capacitance that can be seen as the orange line at $n_0/c = 0$ V. This peak is from the bilayer graphene. The 1D plot is a line cut taken

Figure 5.3: The room temperature (300 K) data taken for KC004 at no external magnetic field (0 T). (a) An optical image of the device. (b) A schematic of the layers of KC004. There is bilayer graphene flake in contact with $MoS₂$ that has been sandwiched on each side by a piece of BN and graphite. (c) A 2D plot with the penetration capacitance (C_p) scaled by the reference capacitance (C_{ref}) of the capacitance bridge as a function of the charge concentration (n_0/c) and the polarization (p_0/c) . The difference between the red and the blue shows the conduction band edge of the $MoS₂$ where the right side of the graph is the conduction band. (d) A line cut taken of the data plotted in (c) taken at $p_0/c = 5$ V.

at $p_0/c = 5$ V. The graphene is the sharp peak, and the sharp decline at $n_0/c = 2$ V is the $MoS₂$ band edge.

We note that there is an asymmetry factor in our software that accounts for the difference in the top and bottom gate geometric capacitance. For plots in figure 5.3 and figure 5.4 the asymmetry factor was changed to reflect the charge density in the bilayer graphene at low temperature. This is the reason the orientation of the band edge for Mo_2 changes between these two data sets.

This data, although not ideal because of the varying capacitance signal of the amplifier, shows that we can resolve both the bilayer graphene and the M_0S_2 flake in the same device.

The last device that was tested for this thesis is JMA003. The optical image of the device and the layer schematic is seen in figure 5.5(a-b). This device is made with bilayer graphene in contact with $MoS₂$.

The first set of data was taken at 2 K with no external magnetic field applied. The 2D plot (figure 5.5(c)) shows the band edge for $MoS₂$ at $n_0/c \approx 1.5$ V. The graphene band gap can be seen as the peak of capacitance at $n_0/c \approx -0.5$ V. A line cut of the plot in panel (d) was taken at $p_0/c = -3$ V. This plot clearly shows the graphene band gap as the maximum at $n_0/c \approx -0.5$ V, and the decline indicates the band edge of the MoS₂.

Figure 5.5(e-f) is the second set of data that was taken after the external magnetic field was applied to the device. The 2D plot shows the integer quantum Hall gaps of the bilayer graphene. These filling factors can be seen as vertical spikes in the capacitance. The filling factors can be seen even more clearly in the 1D plot, which was created by taking a line cut at $p_0/c = -5$ V, as the local maxima.

Figure 5.4: The data taken for KC004 at 2K with no external magnetic field. (a) The data for the scaled capacitance measurements as a function of charge concentration and polarization. The band edge of $MoS₂$ can be seen, but it is vertical. (b) A line cut taken of plot (a) taken at $n_0/c = 5$ V shows that the relationship is linear. (c) The background of plot (a) was subtracted by taking a line cut at $n_0/c = -5$ V and then subtracted from the rest of the lines of the plot. This gives us the expected vertical line of the M_0S_2 and the band edge. The band gap of the bilayer graphene can also be seen as the slight yellow line. (d) A line cut was taken at $p_0/c = 5$ V of plot (c). At $n_0/c = 0$ V, there is a sharp peak from the band gap of the graphene. The red line then declines around $n_0/c = 2$ V indicating the MoS₂ band edge.

Figure 5.5: The data taken for the device JMA003. (a) An optical image of the device with the patterned electrodes. (b) A layer schematic of the device. This device has bilayer graphene in contact with $MoS₂$ that is sandwiched between BN and graphite on both sides. (c) A 2D plot taken at 2 K with no applied magnetic field (0 T). It shows the penetration capacitance scaled by the reference capacitance of the capacitance bridge (C_p/C_{ref}) as a function of the charge concentration (n_0/c) and the polarization (p_0/c) . The band edge of the $MoS₂$ can be seen on the right of the graph, represented by the change in colors from red to blue. (d) A line cut of plot (c) taken at $p_0/c = -3$ V. This shows the band gap of the graphene around $n_0/c = -0.5$ V as the sharp peak. The band edge of the MoS₂ is seen around $n_0/c = 1.5$ V indicated by the decline. (e) C_p/C_{ref} as a function of n_0/c and p_0/c taken for the device at a temperature of 2 K and with an applied magnetic field of 9 T. This plot shows the quantum Hall gaps of the bilayer graphene. (f) A line cut taken of plot (e) at $p_0/c = -5$ V. The local maxima are the quantum Hall gaps of the bilayer graphene.

Chapter 6

Discussion and Future Work

We have shown that we are able to make highly sensitive capacitance measurements of van der Waals heterostructures using several devices. Measurements were taken in monolayer and bilayer graphene devices. Both of the graphene stacks included contact with $MoS₂$. The measurements of these devices were taken at different temperatures with or without an applied magnetic field. The devices that have the external magnetic field show clear integer quantum Hall gaps. In the measurements taken without an applied magnetic field, the band gap of graphene can be seen and the band edge of $MoS₂$ can be confirmed in a few devices.

There are multiple ways in which we can improve on further fabrication and measurement processes. The masking and etching process doesn't produce as clean of results as we would like. With updates to this process, we can create devices with less overlap and more certainty that we are making connections with the pieces of the device that we are wanting. Another thing that needs some perfecting is the capacitance bridge. Some of the measurements were dominated by noise. Rethinking what parts we use and redesigning how we build the capacitance bridge will help us get even better measurement results.

After these improvements are made, we will look at other ways to attempt to observe

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Figure 6.1: The degradation in ambient conditions and passivation of Chromium triiodide(CrI_3). Panel (a-c) are optical images of CrI_3 in ambient conditions taken at (a) 10 minutes, (b) 15 minutes, and (c) 50 minutes. Panel $(d-f)$ are optical images of CrI₃ after being layered by BN taken at (d) 10 minutes, (e) 15 minutes, and (f) 50 minutes in ambient conditions.

these systems. One of these ways is by incorporating a magnetic material. The devices that were used for this these were all made with $MoS₂$ for its strong spin orbit coupling energy, but we would like to see if we would get the same results by using a material that has intrinsic magnetism. Previously, we have done work with chromium tri-iodide $(CrI₃)$, a layered ferromagnetic semiconductor [48, 49]. One of the hardships of using $CrI₃$ is its degradation time in ambient conditions [50, 51]. Figure 6.1(a-c) shows optical images of how quickly it degrades. After 50 minutes, the flake of $CrI₃$ is almost completely dissolved. We were able to successfully passivate $\rm CrI₃$ by covering the area of the flake with BN (figure 6.1(d-f)). Knowing this, we believe that we will be able to fully encapsulate the $CrI₃$ in a stack and prevent it from degrading. We can then repeat the capacitance measurements with $CrI₃$ in place of $MoS₂$.

It has been theorized that stacking graphene in between a material with a strong spin orbit coupling and a material that is intrinsically magnetic will result in a definite QAHE [1]. To achieve these results, we would like to fabricate a device that has bilayer graphene in between a layer of MoS_2 and CrI_3 . With the way the device is fabricated, we hope to fully encapsulate the CrI₃. We would then perform capacitance measurements, in hopes to realize the QAHE.

Appendix

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Curriculum Vitae

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EDUCATION

GRADUATE:

M.Sc. in Physics at University of Nevada, Las Vegas (UNLV) *Current* Thesis topic: Towards highly sensitive capacitance measurements of a quantum anomalous Hall phase in van der Waals heterostructures.

UNDERGRADUATE:

B.Sc. in Physics at University of Nevada, Las Vegas *May 2020* Minor: Mathematics Research: Towards passivation techniques for two-dimensional ferromagnetic chromium tri-iodide.

RESEARCH INTERESTS

My research interests span over the field of condensed matter physics. Specifically, I study materials on the nanoscale. I started my interest for 2-dimensional materials in my undergraduate career where I studied the degradation of materials and the effect on their electronic properties. Currently, I am looking at synthetic topological phases in van der Waals heterostructures.

EXPERIENCE

Graduate Assistant (UNLV) *August 2020 - present*

- Instruction of intro-level physics labs.

ACHIEVEMENTS

Graduate Assistantship (UNLV) *Fall 2020 - Spring 2022* Society of Physics Students member (UNLV) *2017-2020* Dean's Honor List (UNLV) *Spring 2020, Fall 2019* Dean's List (College of Southern Nevada) *Spring 2016, Spring 2015, Fall 2016*

PERSONAL NOTE

Outside of academia, I enjoy fitness and getting outdoors. I am constantly looking for a good hike or adventure with my husband and dog.

PUBLICATIONS

(1) Haley, K.L.; Cloninger, J.A.; Cerminara, K.; Sterbentz, R.M.; Taniguchi, T.; Watanabe, K.; Island, J.O. Heated Assembly and Transfer of Van der Waals Heterostructures with Common Nail Polish. https://doi.org/10.3390/nanomanufacturing1010005*Nanomanufacturing* 1, 49-56 (2021).